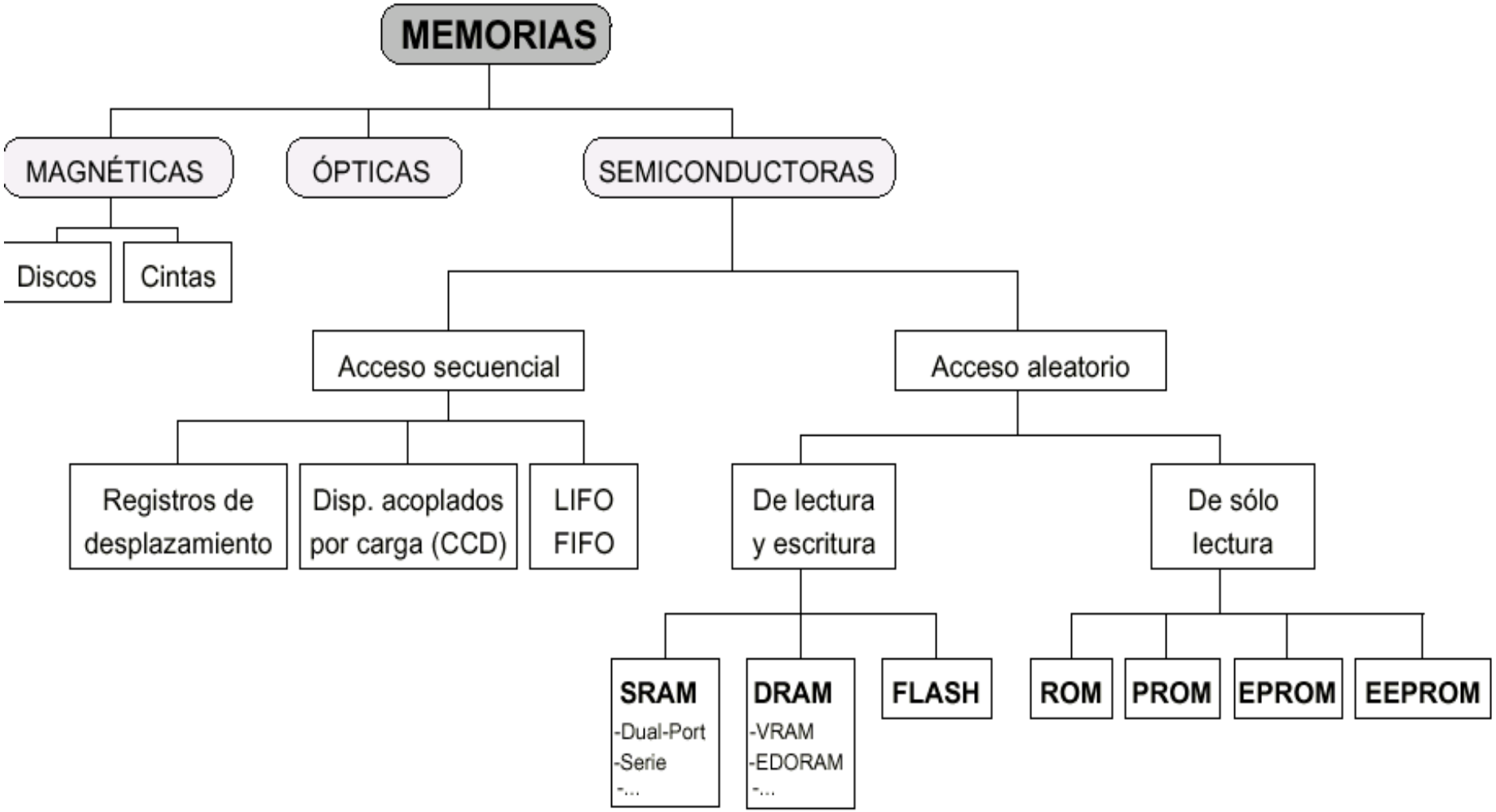
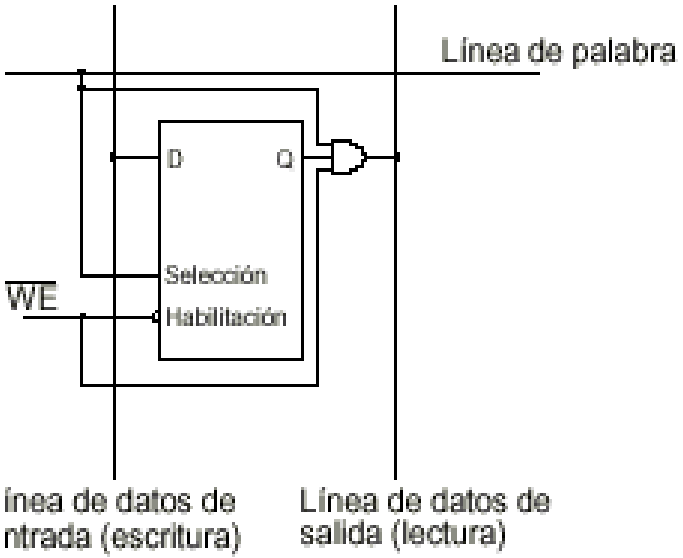
Clasificación de memorias



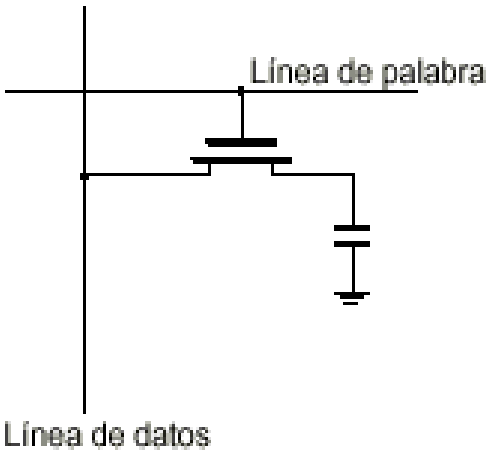
Características de las memorias semiconductoras de acceso aleatorio

Celdas básicas de las memorias semiconductoras

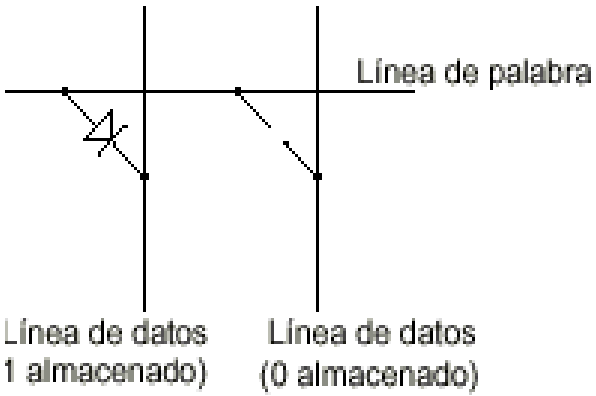
SRAM



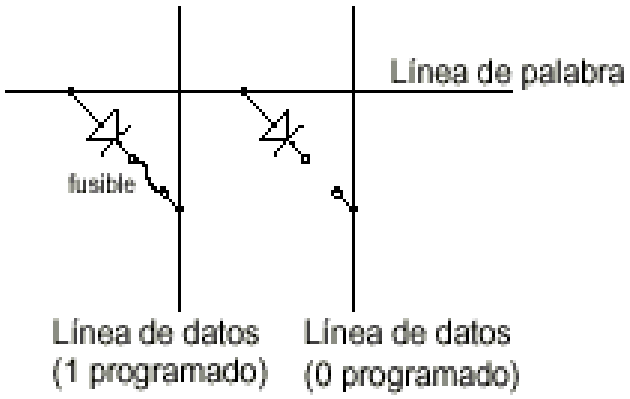
DRAM

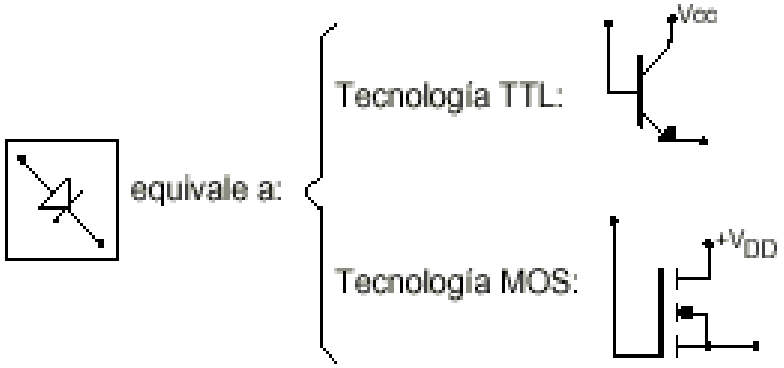


ROM

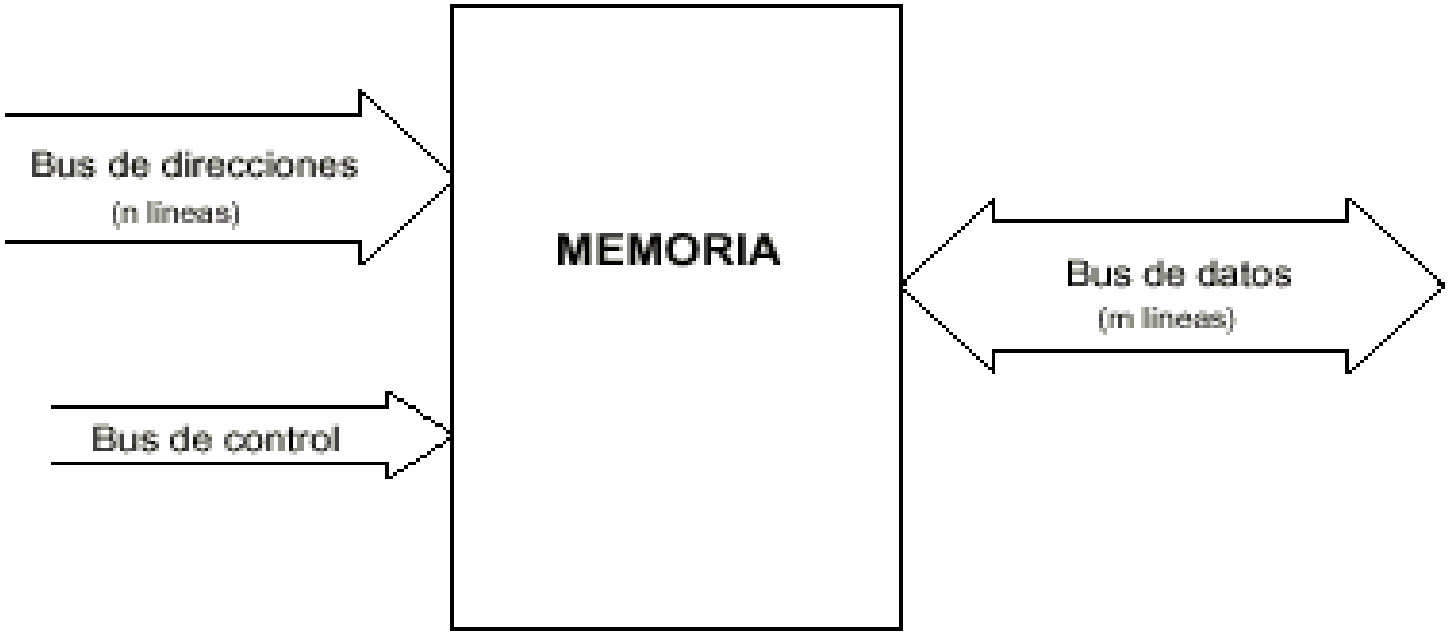


PROM





Organización y capacidad de una memoria

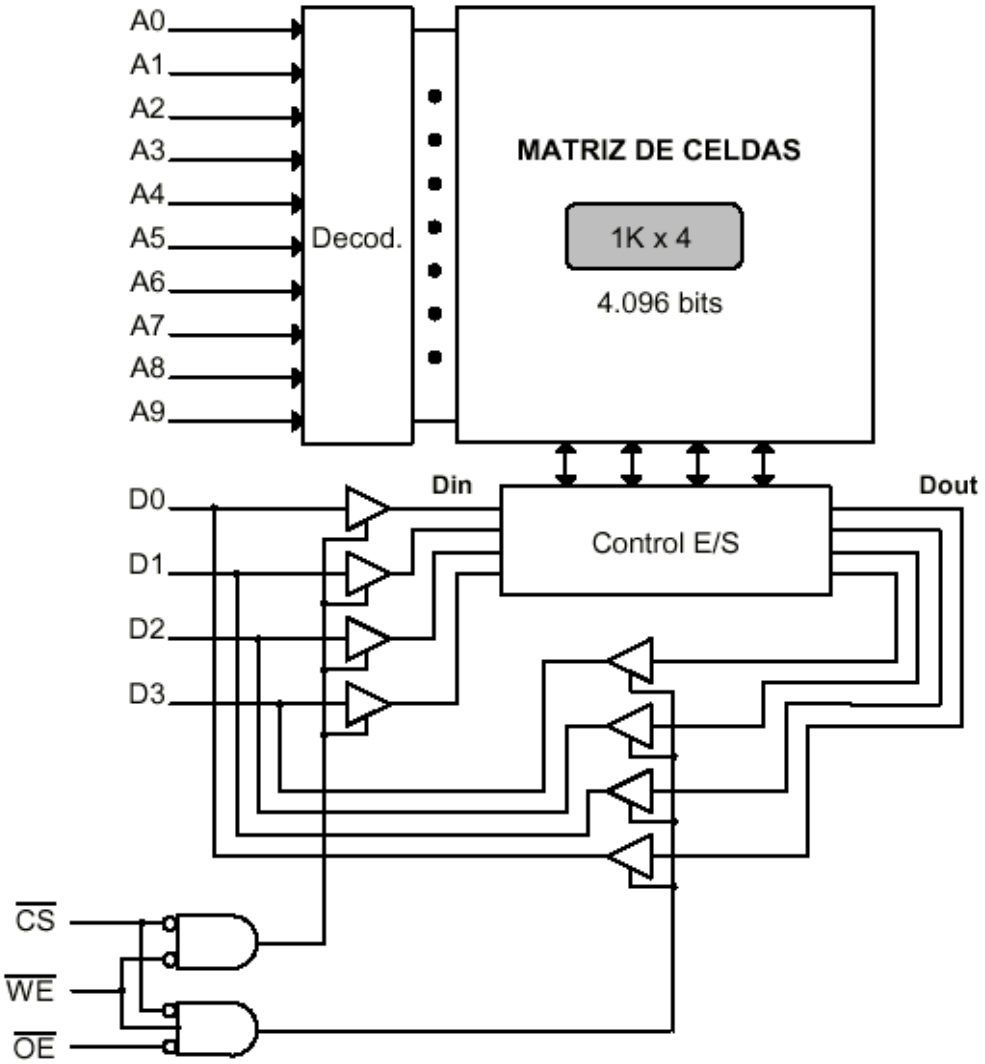


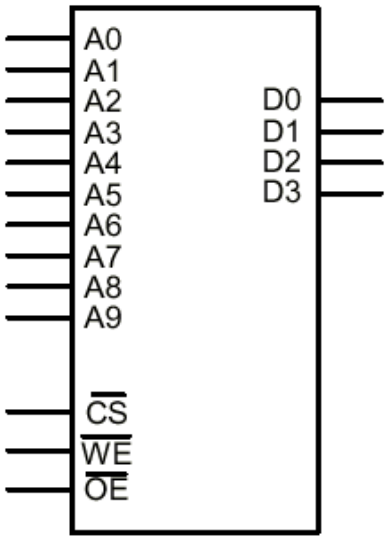
Nº de palabras: 2^n

Bits/palabra: m

→ Organización: 2^n x m bits

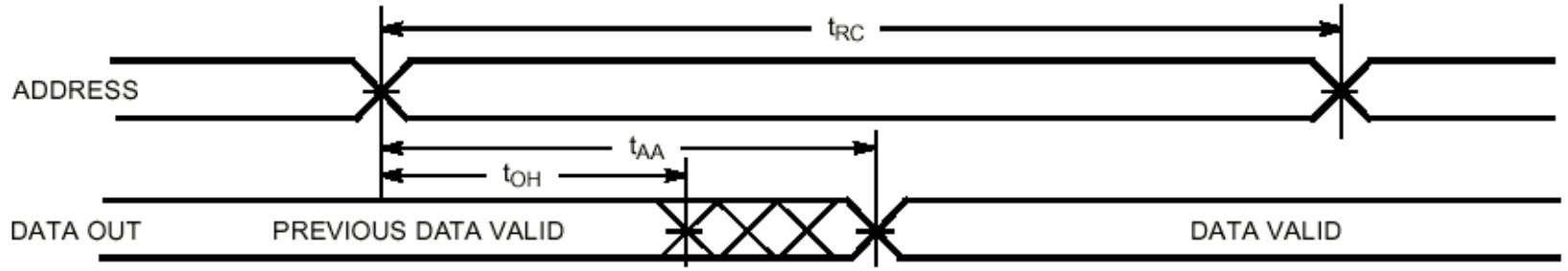
Estructura interna de una memoria RAM estática



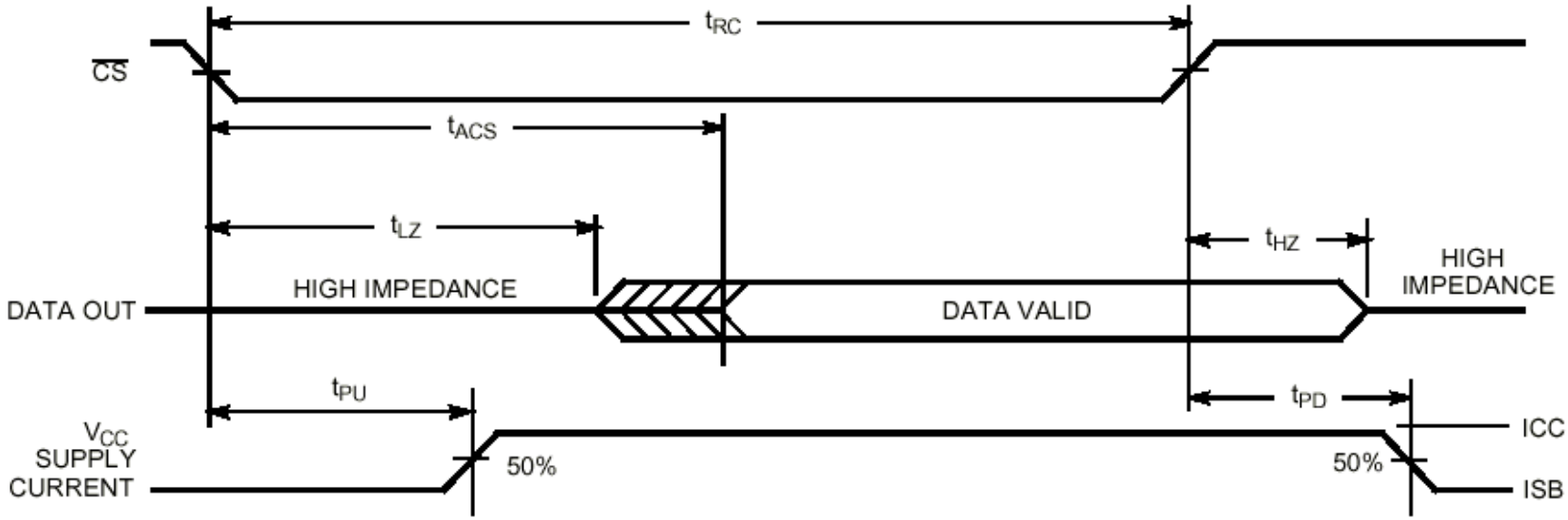


Ciclos de lectura (Memoria RAM estática CY7C148)

Read Cycle No. 1 [10,11]



Read Cycle No. 2 [10,12]

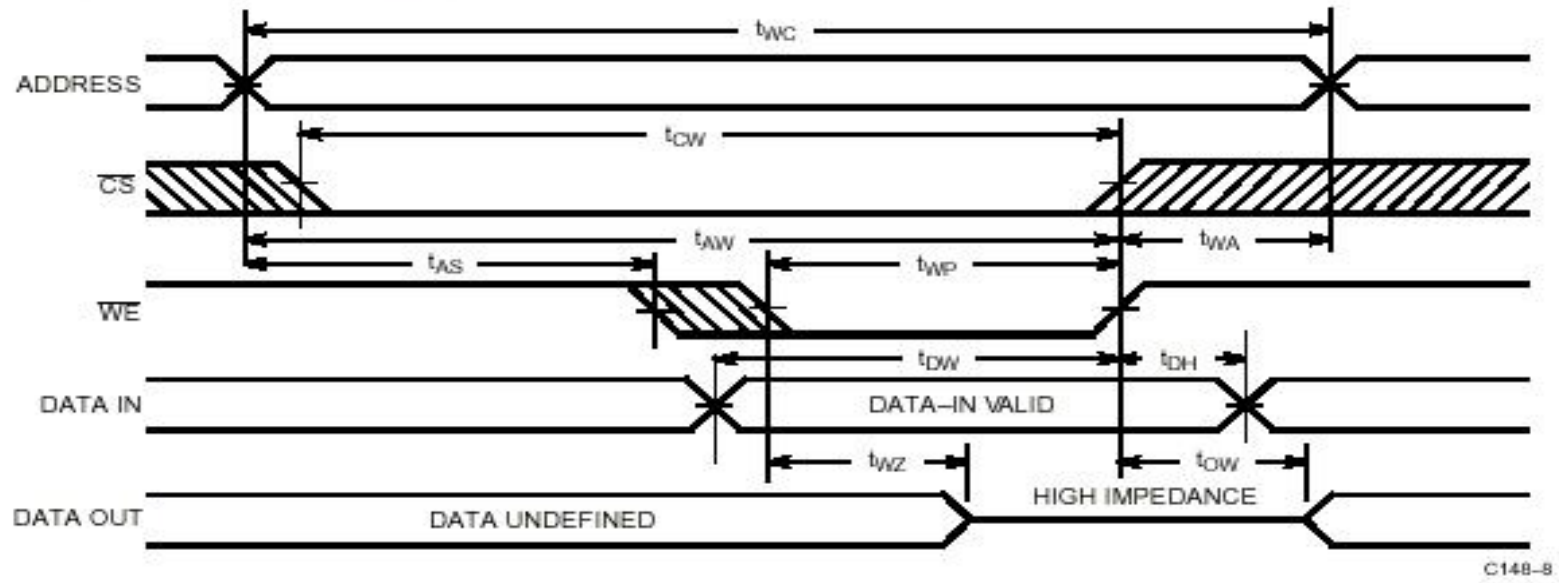


Notes:

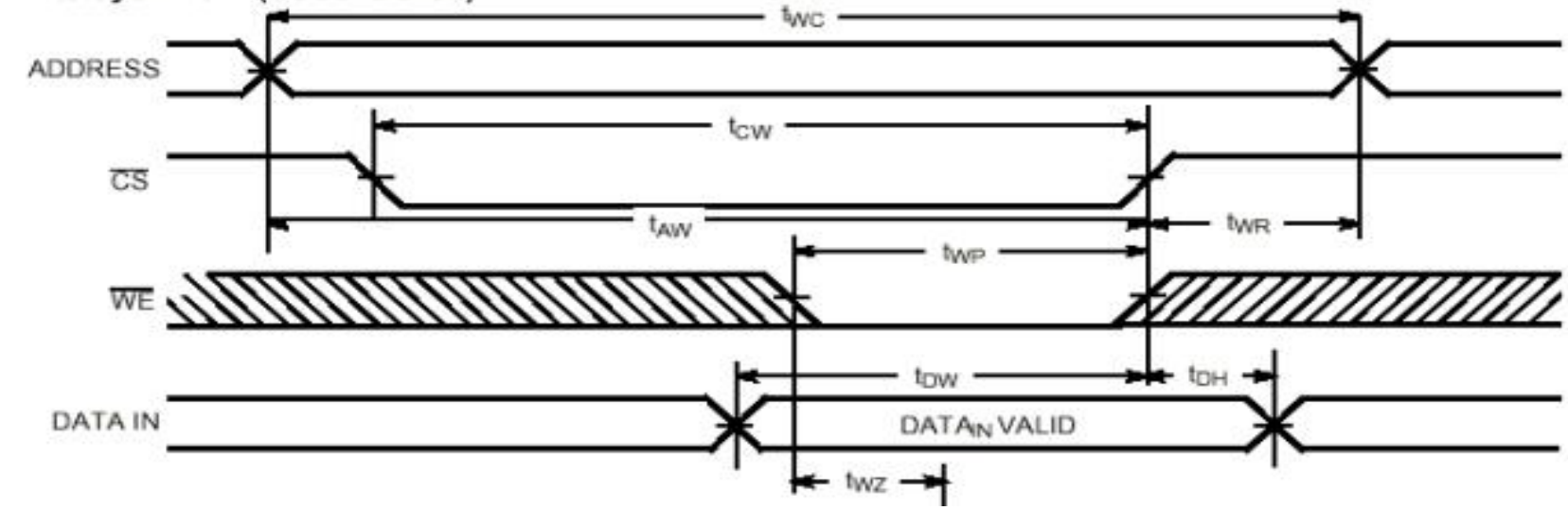
10. $\overline{WE}$ is HIGH for read cycle.
11. Device is continuously selected, $\overline{CS} = V_{IL}$.
12. Address valid prior to or coincident with $\overline{CS}$ transition LOW.

Ciclos de escritura (Memoria RAM estática CY7C148)

Write Cycle No. 1 ($\overline{WE}$ Controlled)



Write Cycle No. 2 ($\overline{CS}$ Controlled)[13]



Características temporales de la memoria

Switching Characteristics Over the Operating Range[2]

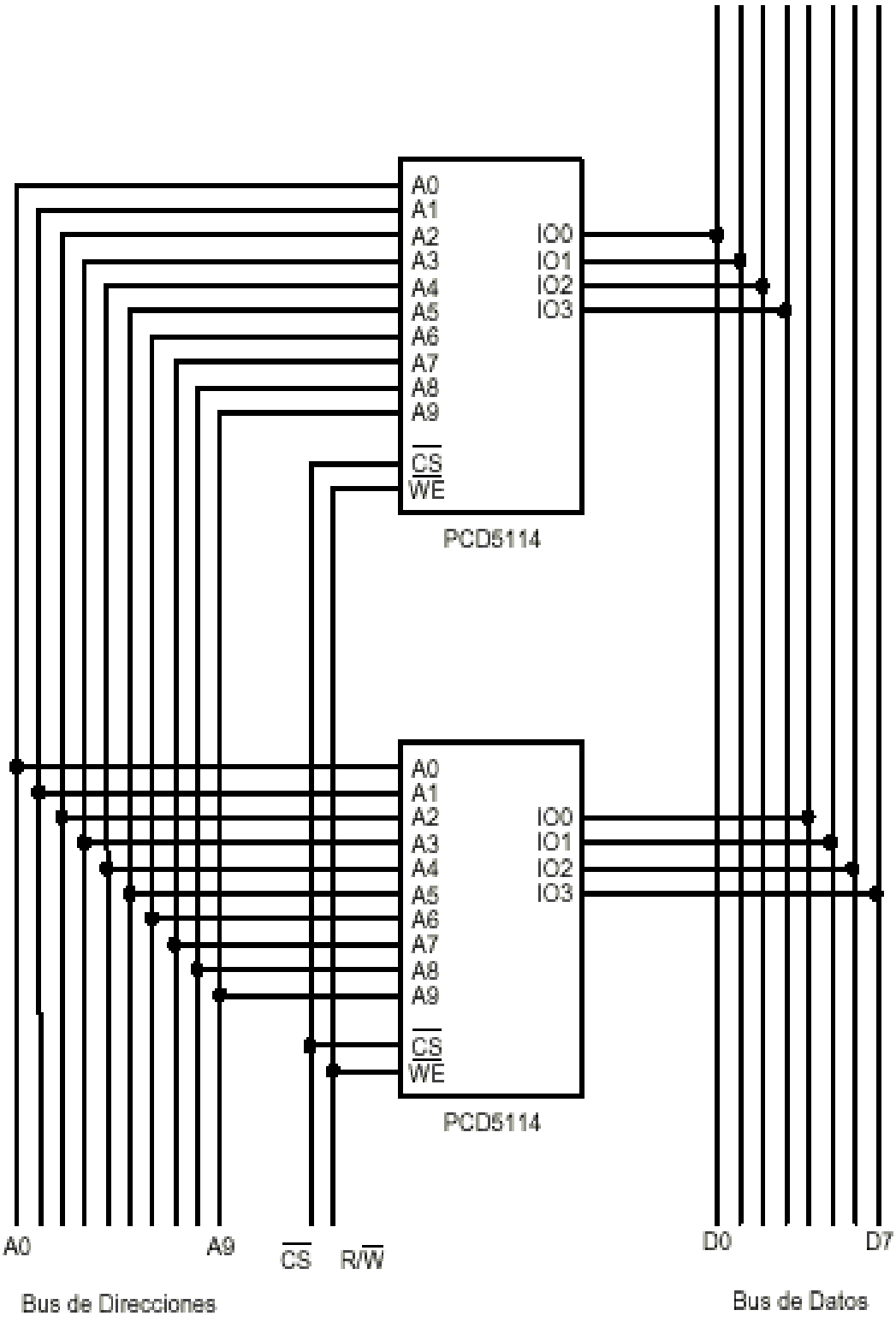
Parameter	Description		7C148–25 7C149–25		7C148–35 7C149–35		7C148–45 7C149–45		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE									
t_{RC}	Address Valid to Address Do Not Care Time (Read Cycle Time)		25		35		45		ns
t_{AA}	Address Valid to Data Out Valid Delay (Address Access Time)			25		35		45	ns
t_{ACS1} t_{ACS2}	Chip Select LOW to Data Out Valid (7C148 only)			25[6]		35		45	ns
				30[7]		35		45	ns
t_{ACS}	Chip Select LOW to Data Out Valid (7C149 only)			15		15		20	ns
t_{LZ}[8]	Chip Select LOW to Data Out On	7C148	8		10		10		ns
		7C149	5		5		5		
t_{HZ}[8]	Chip Select HIGH to Data Out Off		0	15	0	20	0	20	ns
t_{OH}	Address Unknown to Data Out Unknown Time		0		0		5		ns
t_{PD}	Chip Select HIGH to Power-Down Delay	7C148		20		30		30	ns
t_{PU}	Chip Select LOW to Power-Up Delay	7C148	0		0		0		ns
WRITE CYCLE									
t_{WC}	Address Valid to Address Do Not Care (Write Cycle Time)		25		35		45		ns
t_{WP}[9]	Write Enable LOW to Write Enable HIGH		20		30		35		ns
t_{WR}	Address Hold from Write End		5		5		5		ns
t_{WZ}[8]	Write Enable to Output in High Z		0	8	0	8	0	8	ns
t_{DW}	Data in Valid to Write Enable HIGH		12		20		20		ns
t_{DH}	Data Hold Time		0		0		0		ns
t_{AS}	Address Valid to Write Enable LOW		0		0		0		ns
t_{CW}[9]	Chip Select LOW to Write Enable HIGH		20		30		40		ns
t_{OW}[8]	Write Enable HIGH to Output in Low Z		0		0		0		ns
t_{AW}	Address Valid to End of Write		20		30		35		ns

Notes:

6. Chip deselected greater than 25 ns prior to selection.
7. Chip deselected less than 25 ns prior to selection.
8. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for all devices. Transition is measured ±500 mV from steady-state voltage with specified loading in part (b) of AC Test Loads.
9. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going high. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

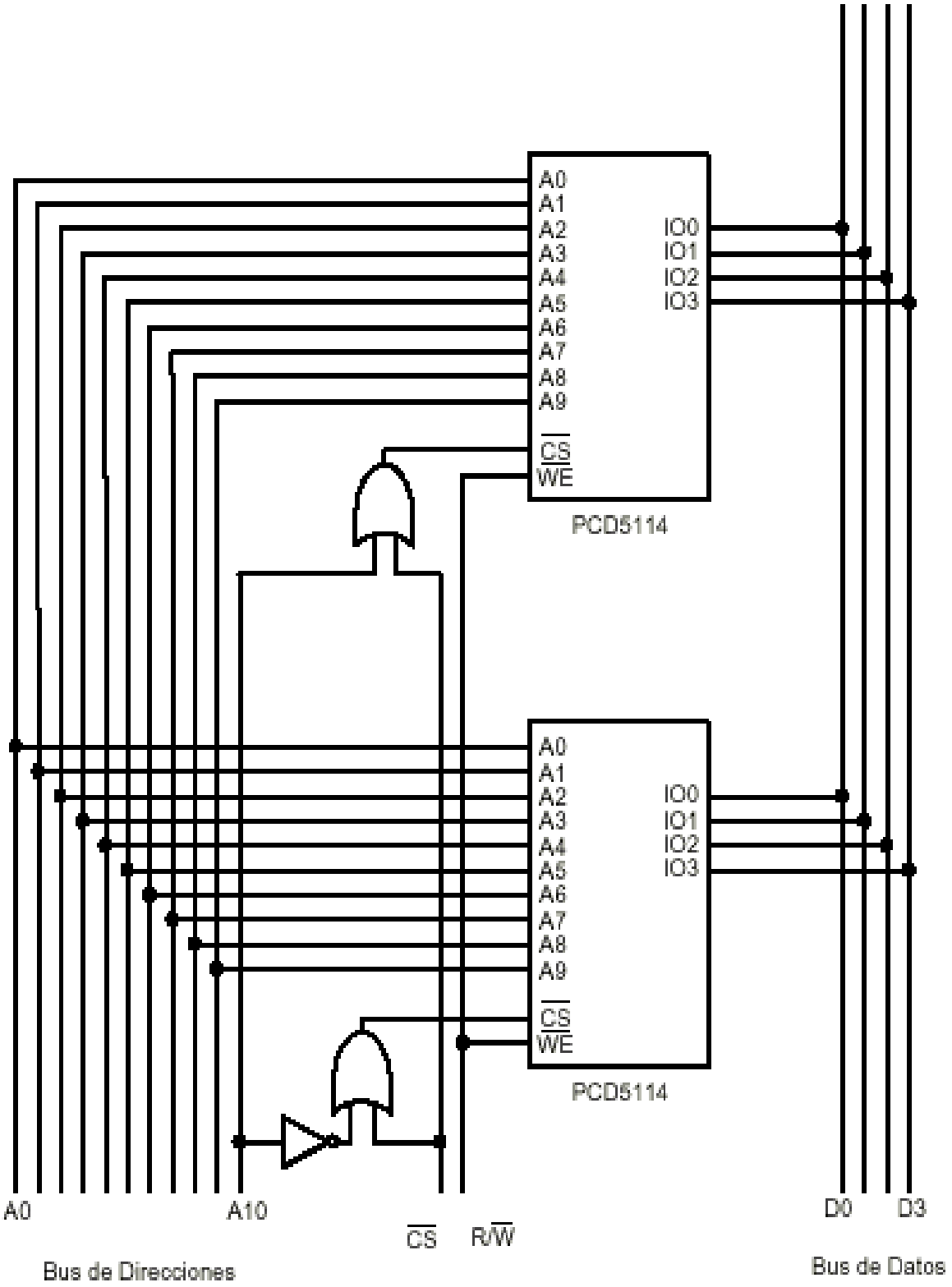
Ampl. de la longitud de palabra de una memoria

2 chips PCD5114 (1k x 4) ⟶ Memoria 1k x 8



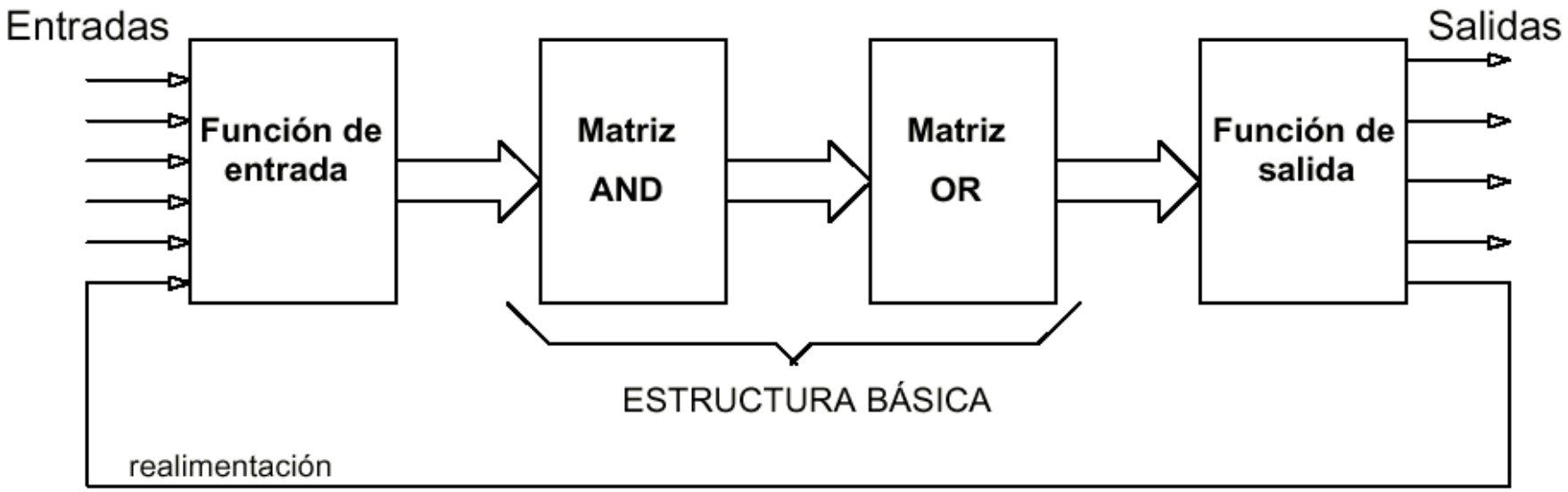
Ampl. del número de palabras de una memoria

2 chips PCD5114 (1k x 4) ⟶ Memoria 2k x 4



Dispositivos de Lógica Programable (PLDs)

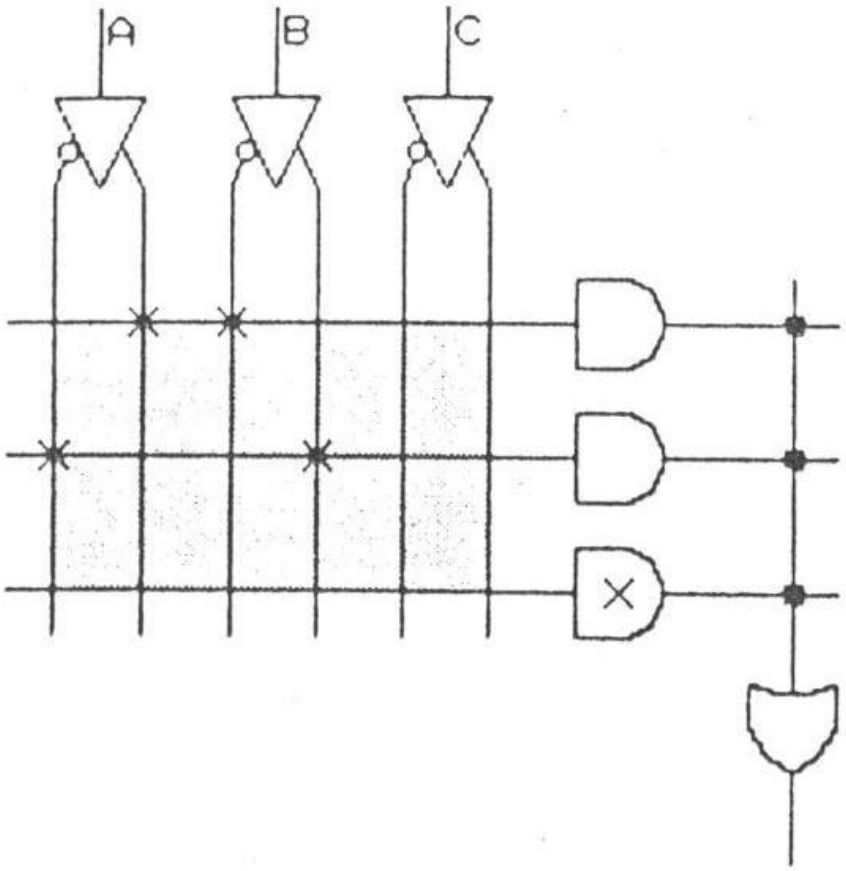
Estructura general de un PLD



Tipos:

- PROM
- PAL – GAL
- FPGA-PLA

Realización de una función lógica con un PLD

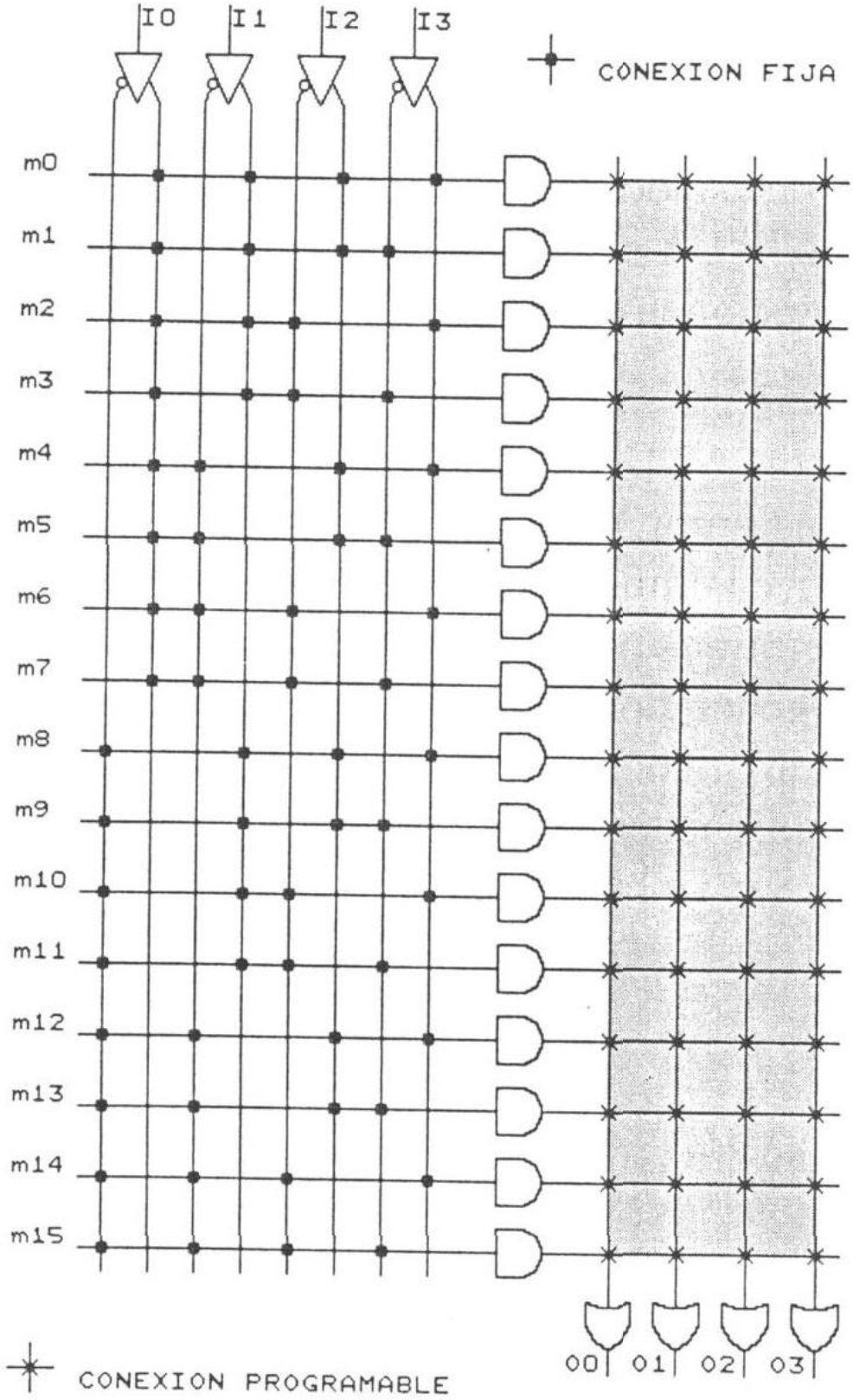


CONEXION FIJA

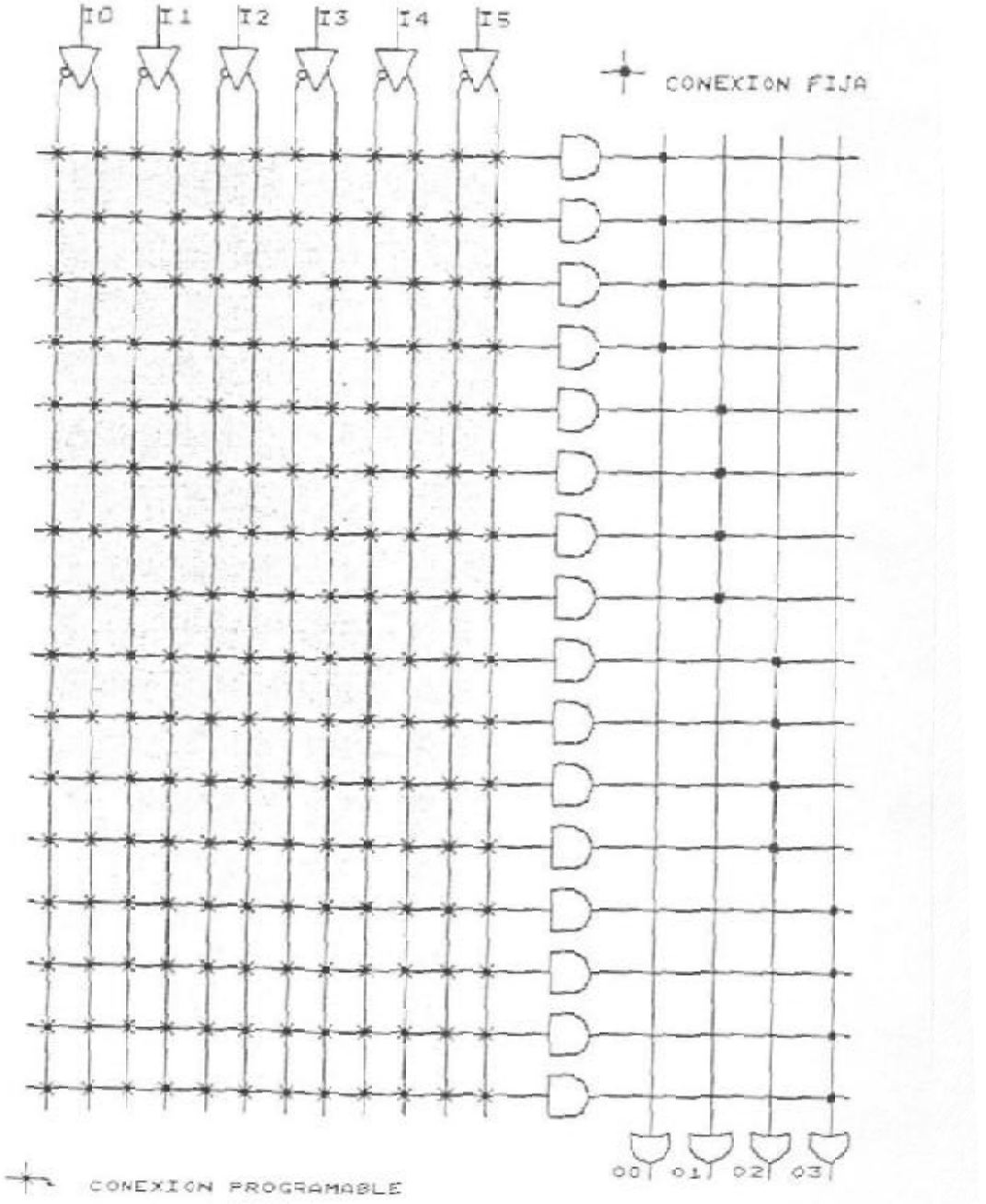
CONEXION PROGRAMABLE

F = A & B' * A' & B

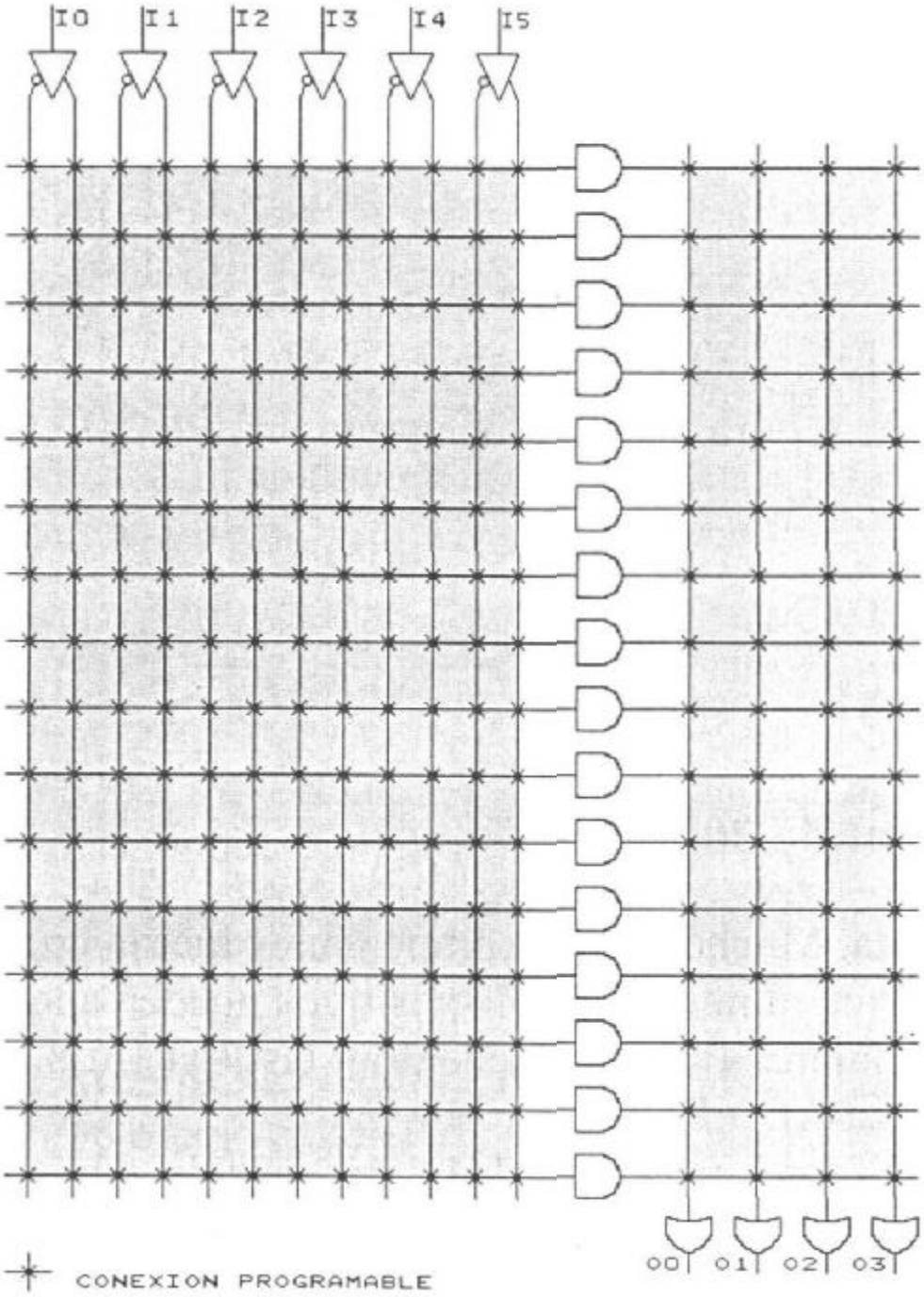
PROM


I0
I1
I2
I3
CONEXION FIJA
m0
m1
m2
m3
m4
m5
m6
m7
m8
m9
m10
m11
m12
m13
m14
m15
O0
O1
O2
O3
CONEXION PROGRAMABLE

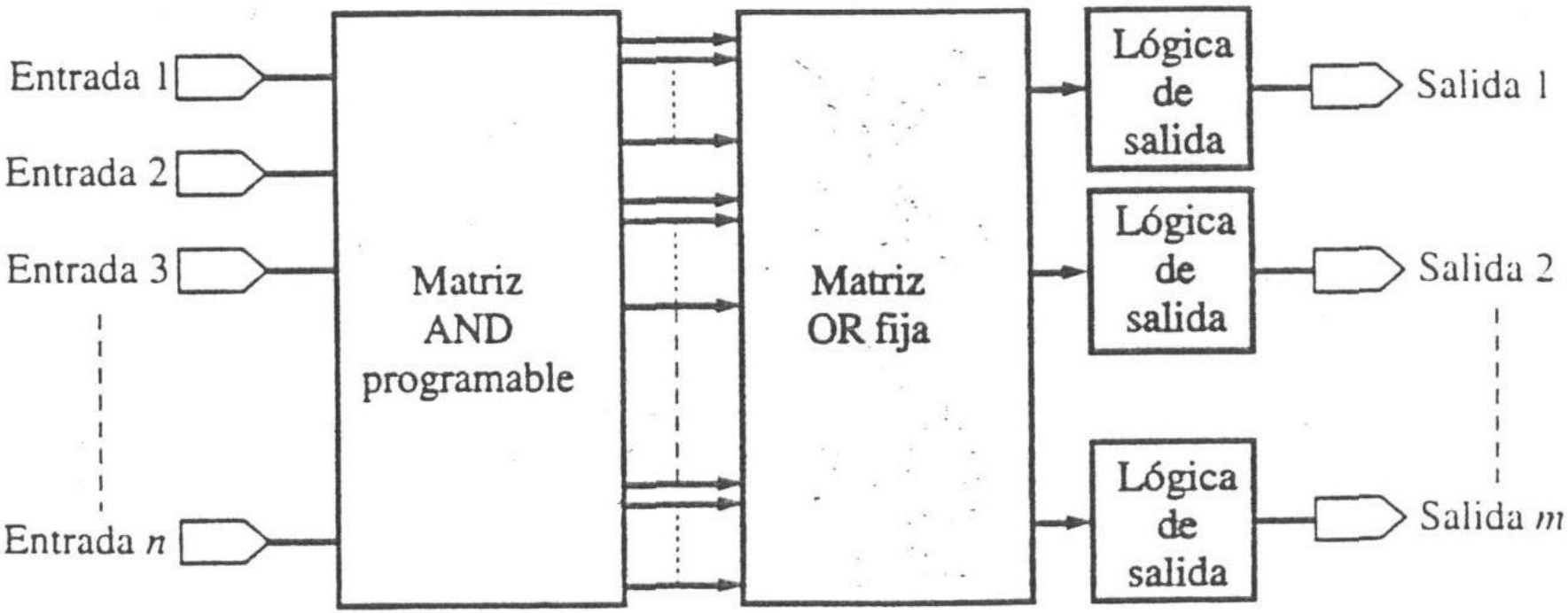
PAL

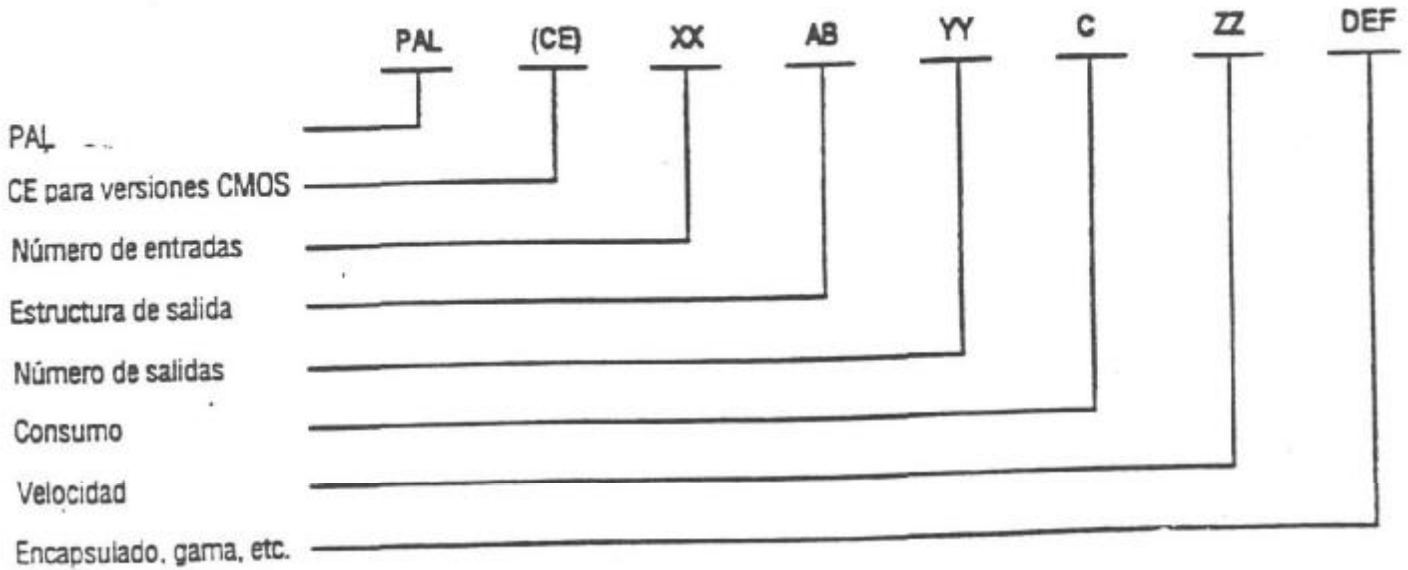

I0
I1
I2
I3
I4
I5
CONEXION FIJA
O0
O1
O2
O3
CONEXION PROGRAMABLE

FPLA



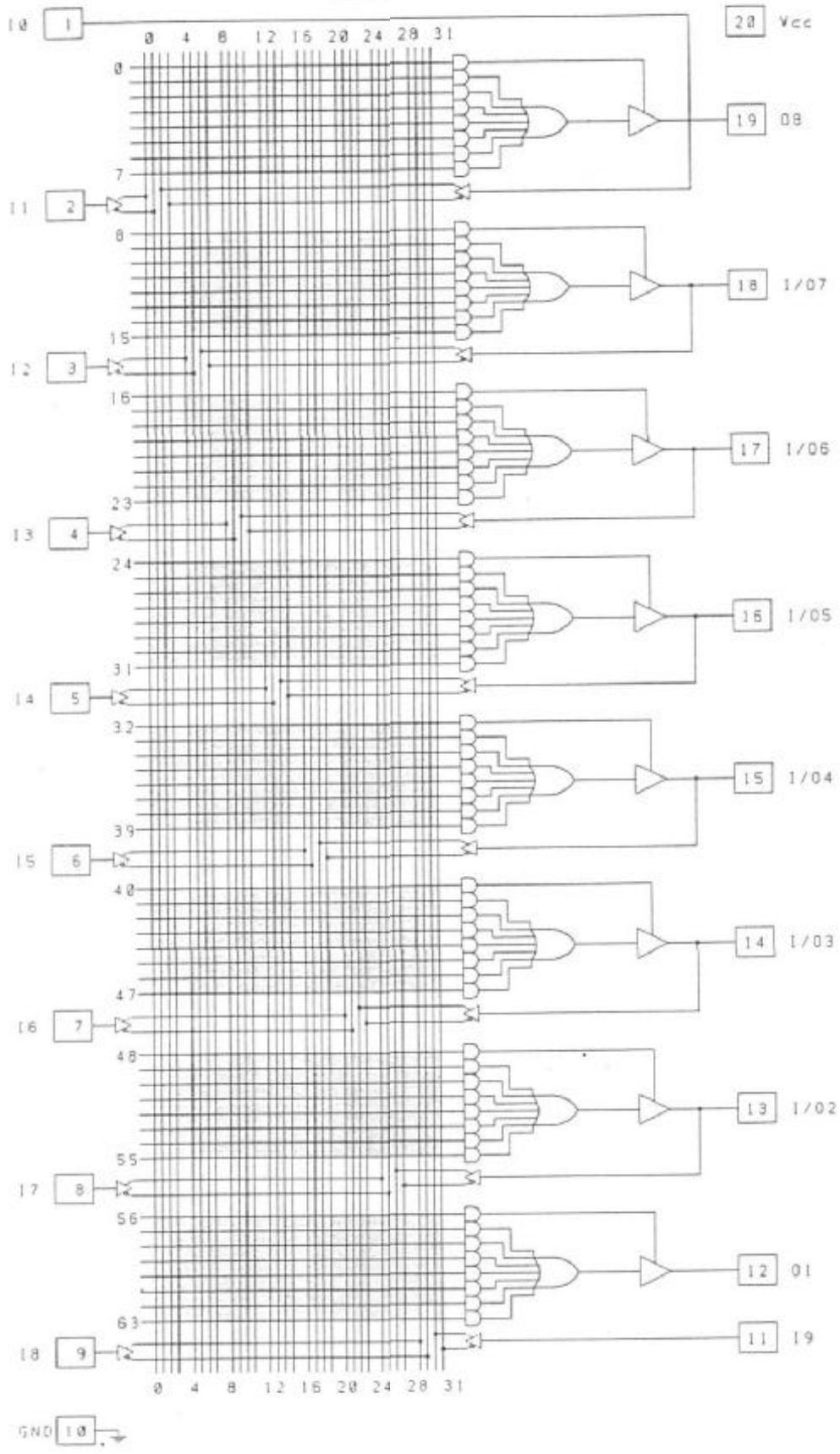
Estructura de una una PAL



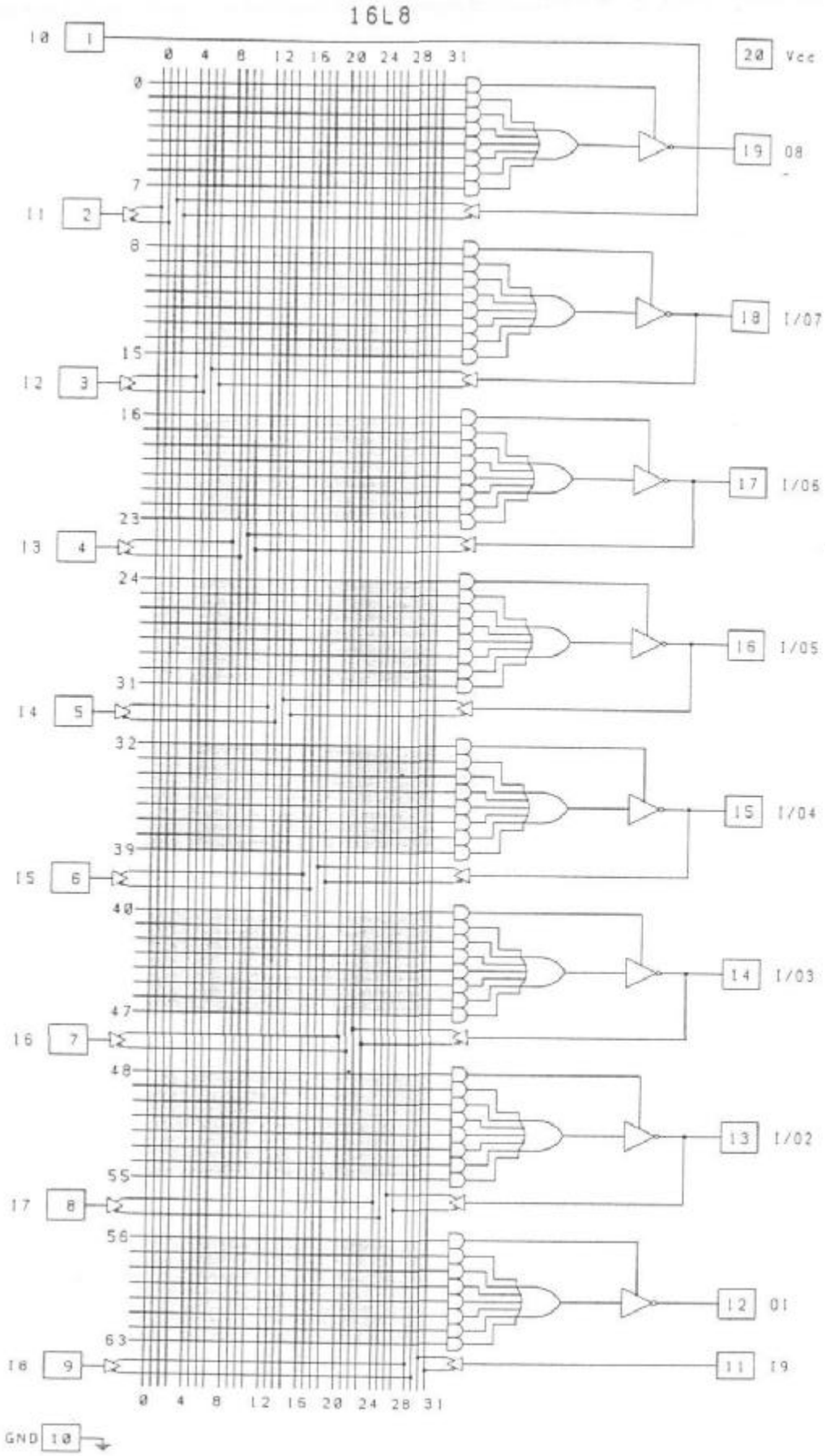


Letra(s) código(s)	Estructura de salida
L	Combinatoria activo bajo
H	Combinatoria activo alto
R	Registro
RA	Registro asíncrono
X	Registro de O exclusivo
V	Versátil

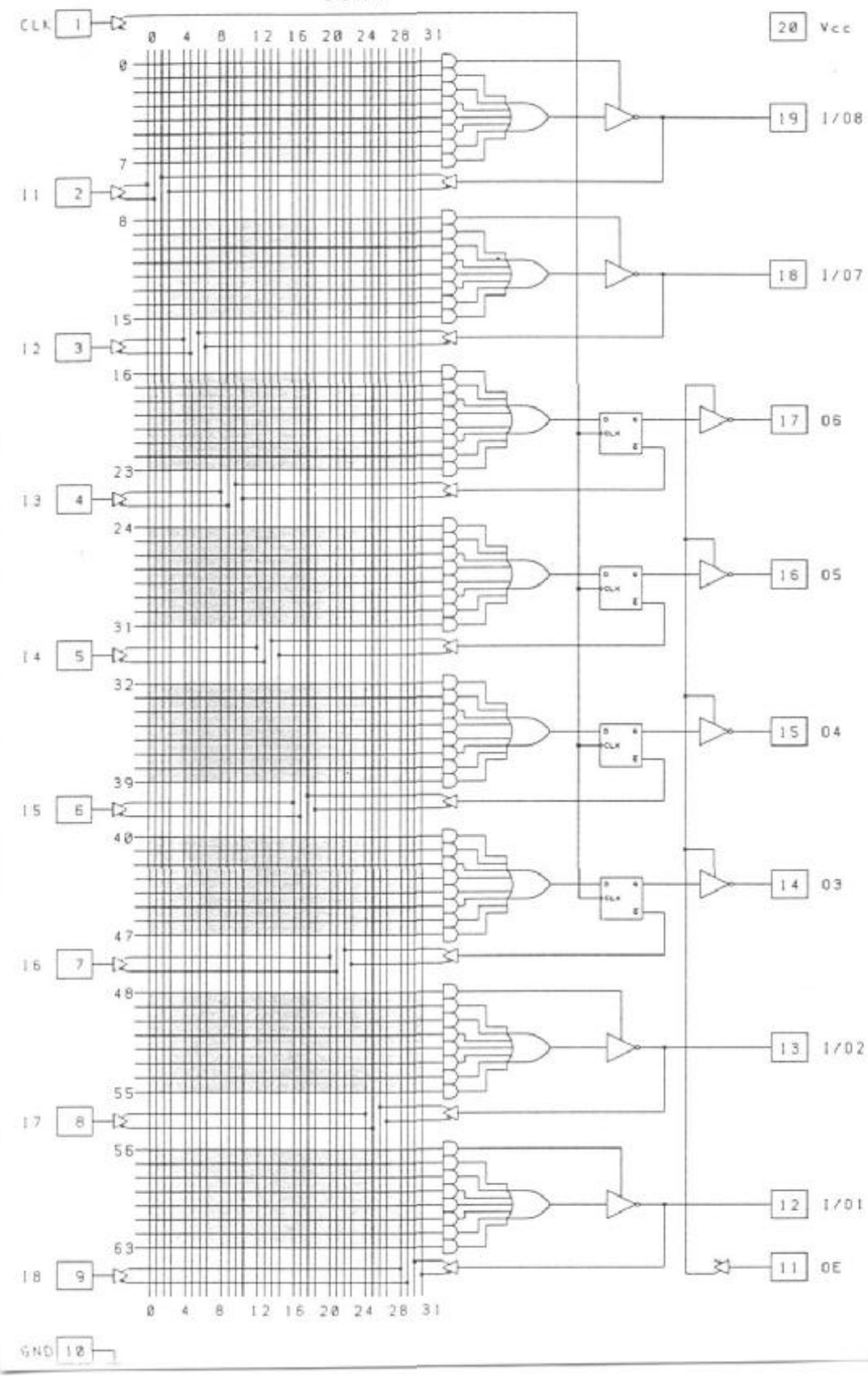
16H8


I0 1
0 4 8 12 16 20 24 28 31
0
7
I1 2
8
15
I2 3
16
23
I3 4
24
31
I4 5
32
39
I5 6
40
47
I6 7
48
55
I7 8
56
63
I8 9
0 4 8 12 16 20 24 28 31
GND 10
20 Vcc
19 O8
18 I/O7
17 I/O6
16 I/O5
15 I/O4
14 I/O3
13 I/O2
12 O1
11 I9

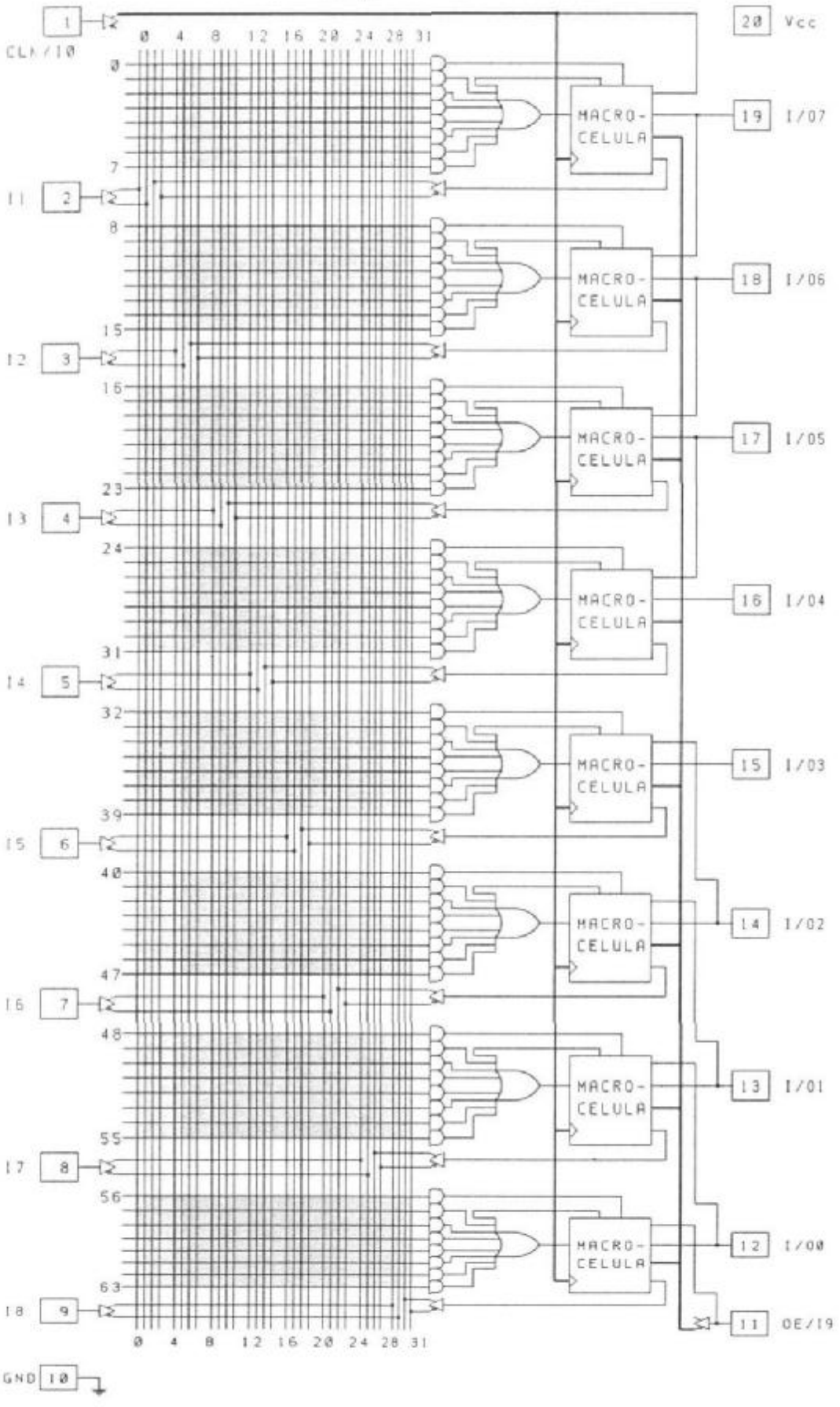
16L8


I0 1
0 4 8 12 16 20 24 28 31
20 Vcc
0
19 O8
7
I1 2
8
18 I/O7
15
I2 3
16
17 I/O6
23
I3 4
24
16 I/O5
31
I4 5
32
15 I/O4
39
I5 6
40
14 I/O3
47
I6 7
48
13 I/O2
55
I7 8
56
12 O1
63
I8 9
11 I9
0 4 8 12 16 20 24 28 31
GND 10

16R4


CLK 1
I1 2
I2 3
I3 4
I4 5
I5 6
I6 7
I7 8
I8 9
GND 10
20 Vcc
19 I/O8
18 I/O7
17 O6
16 O5
15 O4
14 O3
13 I/O2
12 I/O1
11 OE
0 4 8 12 16 20 24 28 31
0
7
8
15
16
23
24
31
32
39
40
47
48
55
56
63

16V8


1
CLK/I0
0 4 8 12 16 20 24 28 31
0
7
11
2
8
15
12
3
16
23
13
4
24
31
14
5
32
39
15
6
40
47
16
7
48
55
17
8
56
63
18
9
0 4 8 12 16 20 24 28 31
GND 10
20 Vcc
MACRO-CELULA
19 I/07
MACRO-CELULA
18 I/06
MACRO-CELULA
17 I/05
MACRO-CELULA
16 I/04
MACRO-CELULA
15 I/03
MACRO-CELULA
14 I/02
MACRO-CELULA
13 I/01
MACRO-CELULA
12 I/00
11 OE/I9

Estructura de la macrocélula en una PAL22V10