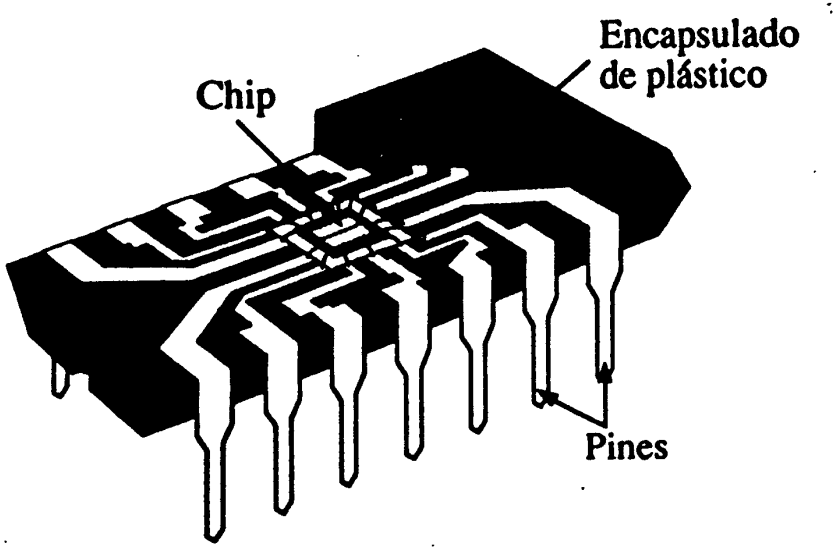
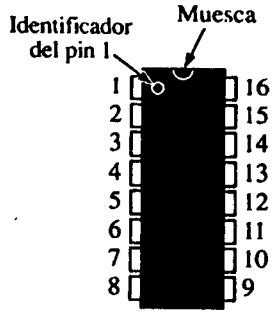
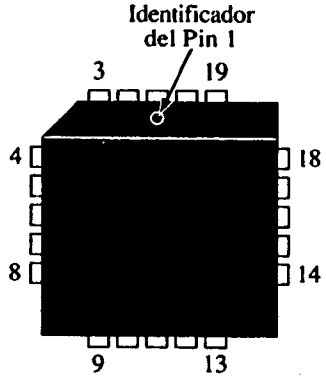
Circuito Digital Integrado



Numeración de los Pines

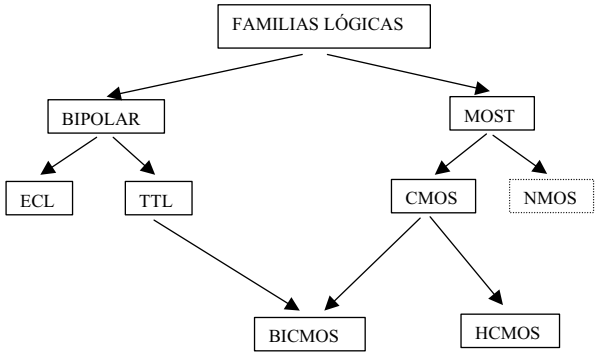


DIP o SOIC



PLCC o LCCC

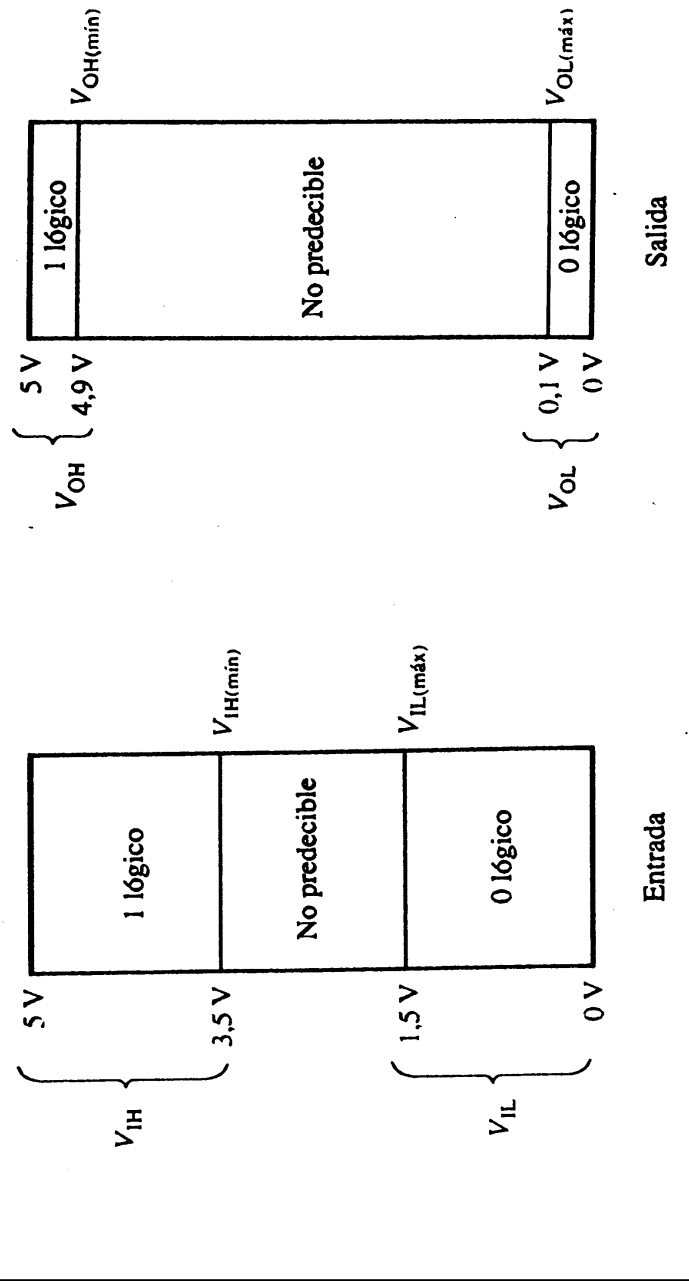
Tecnologías de Circuitos Integrados



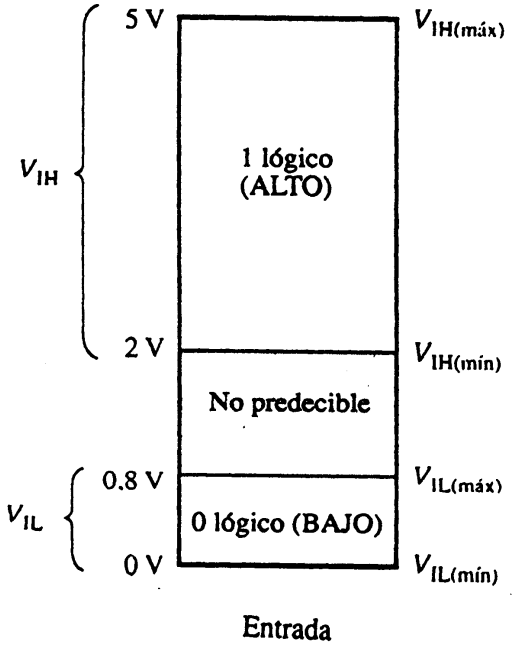
Escalas de Integración

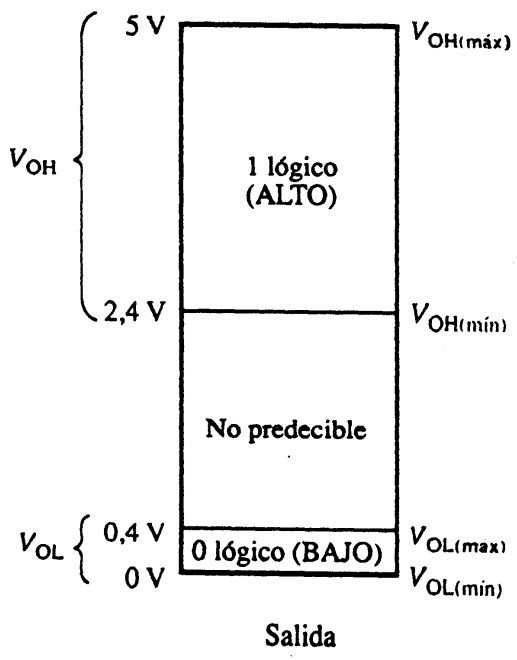
SSI < 12 puertas
MSI < 100 puertas
LSI < 1000 puertas
VLSI > 1000 puertas

Niveles lógicos TTL



Niveles lógicos CMOS

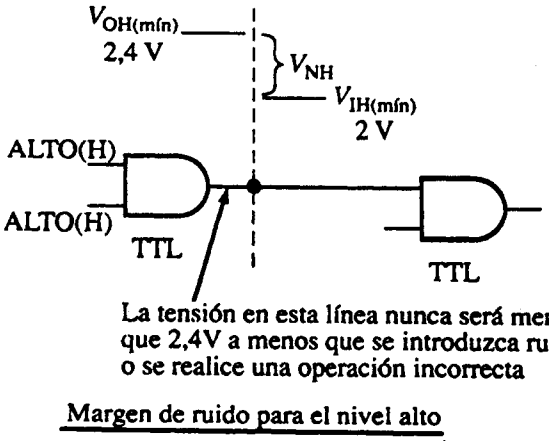


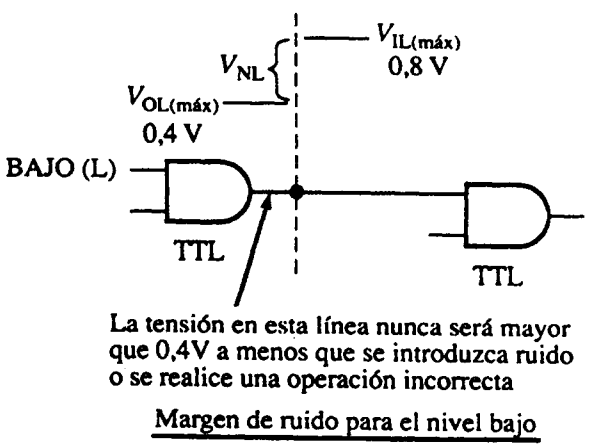


Margen de ruido

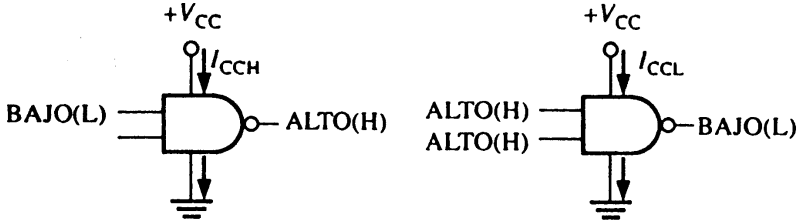
$$V_{NH} = V_{OH(mín)} - V_{IH(mín)}$$

$$V_{NL} = V_{IL(máx)} - V_{OL(máx)}$$



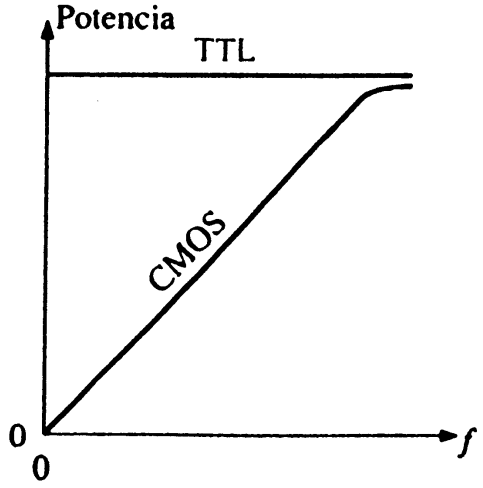


Disipación de Potencia

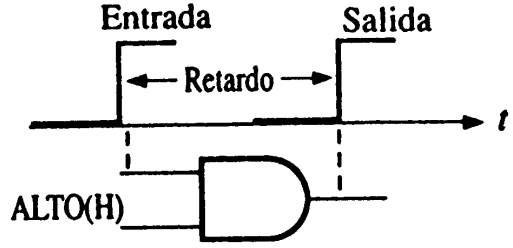


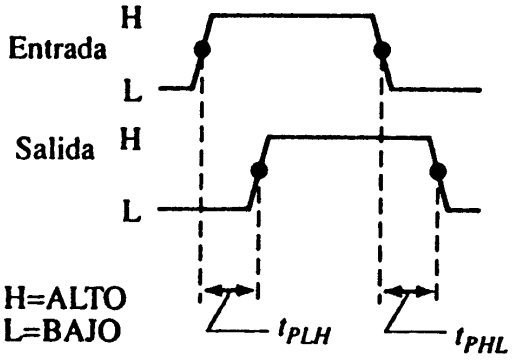
$$I_{CC} = \frac{I_{CCH} + I_{CCL}}{2}$$

$$P_D = V_{CC} I_{CC}$$

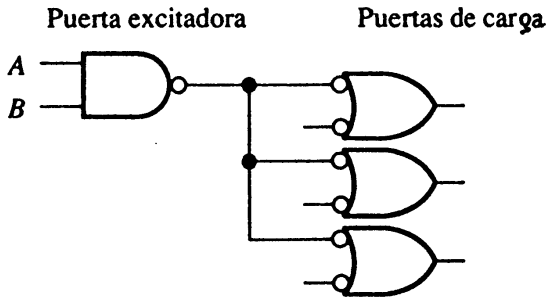


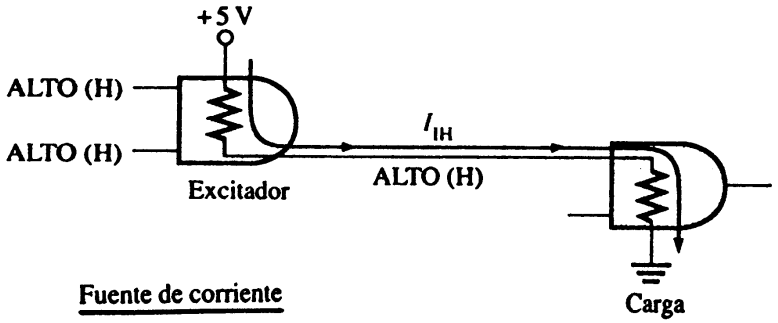
Retardo de propagación



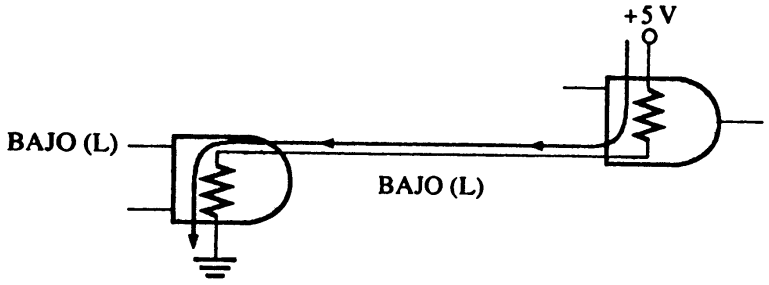


Carga y Fan-out



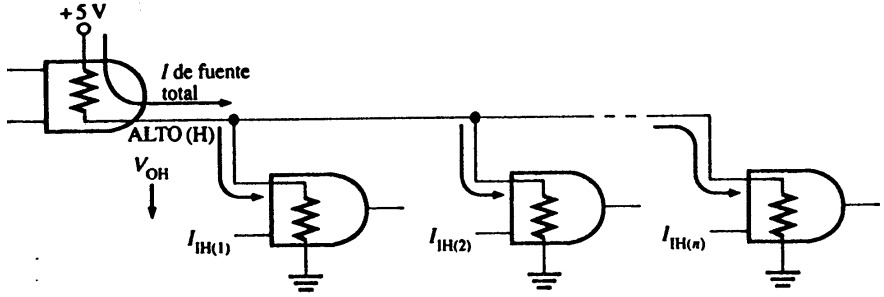


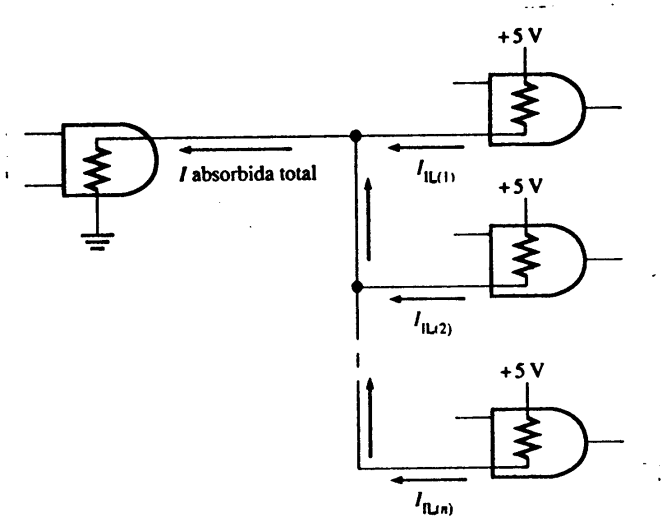
Fuente de corriente



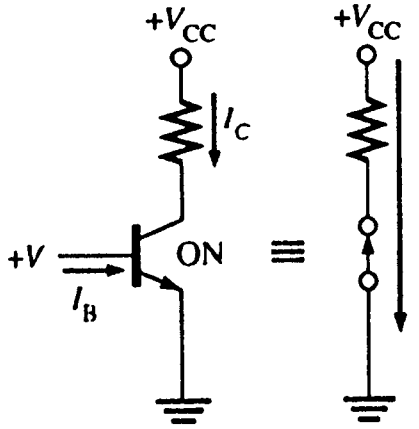
Sumidero de corriente

Carga TTL

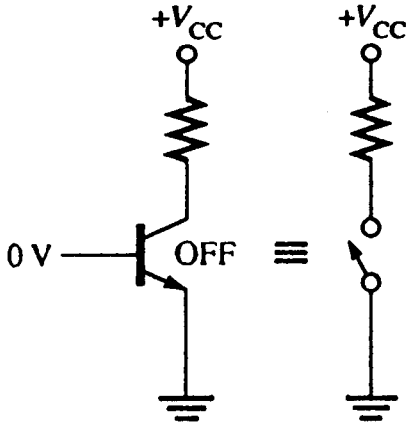




Conmutación del BJT

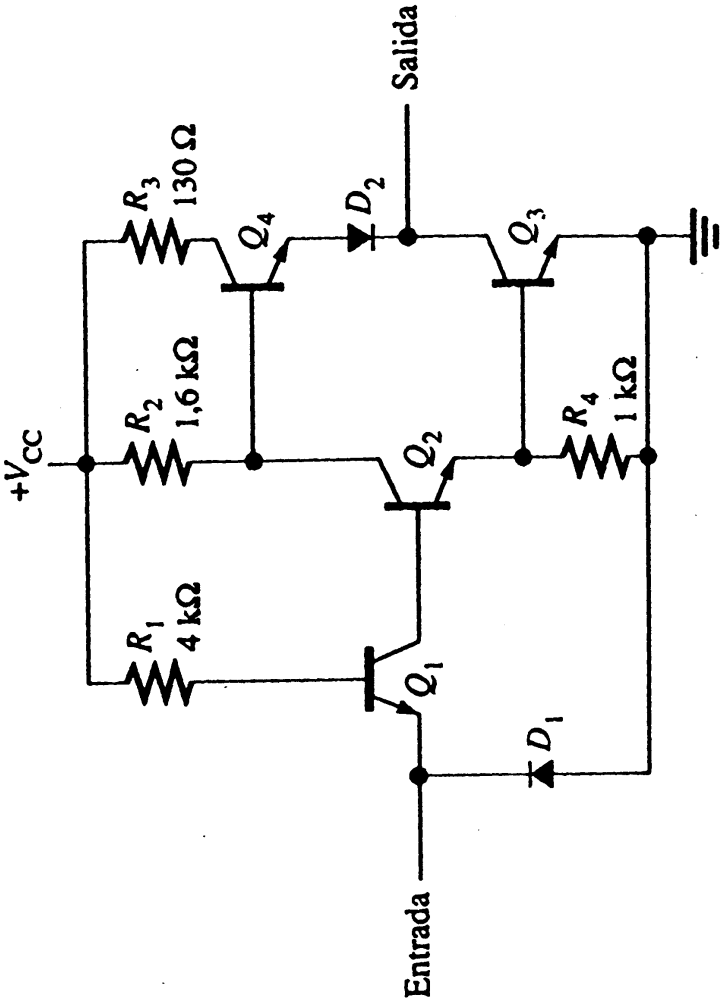


Transistor saturado. Equivale a un interruptor cerrado

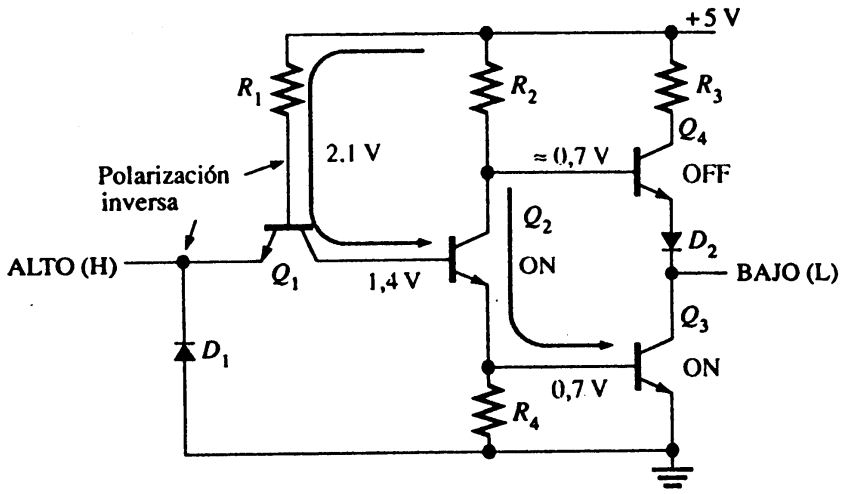


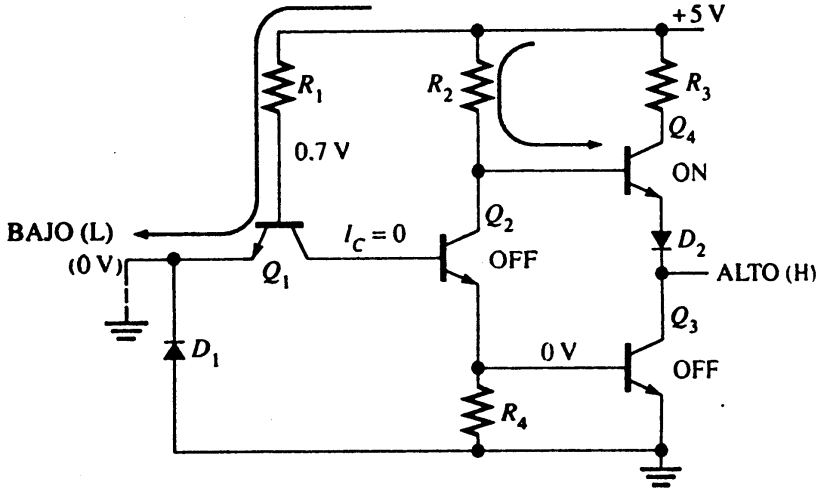
Transistor bloqueado. Equivale a un interruptor abierto

Inversor TTL

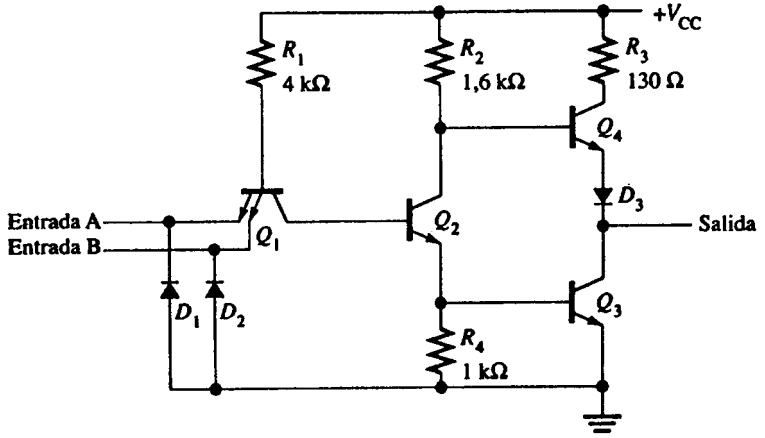


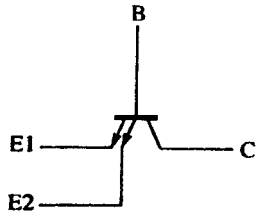
Funcionamiento de un inversor TTL

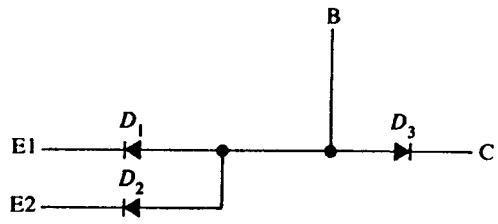




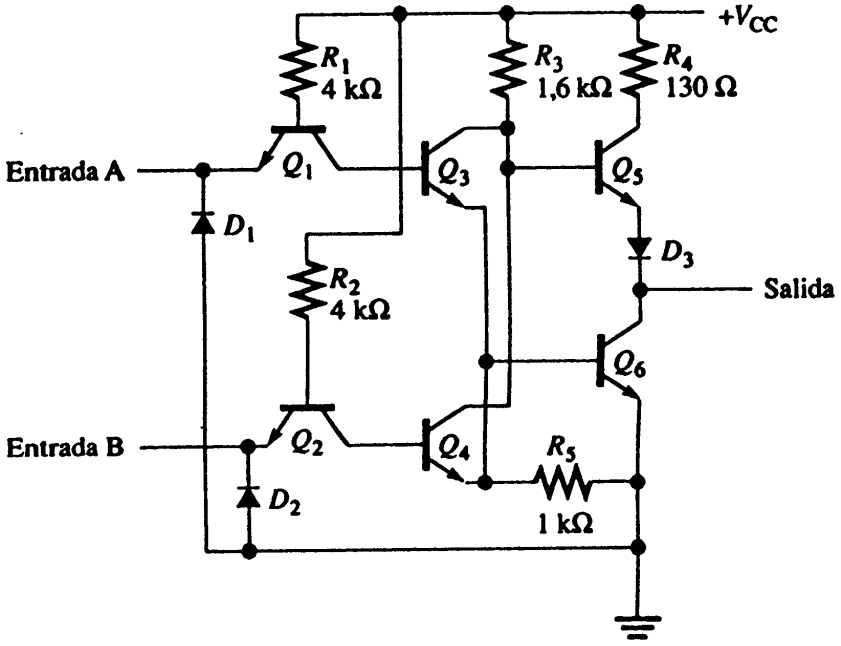
Puerta NAND TTL



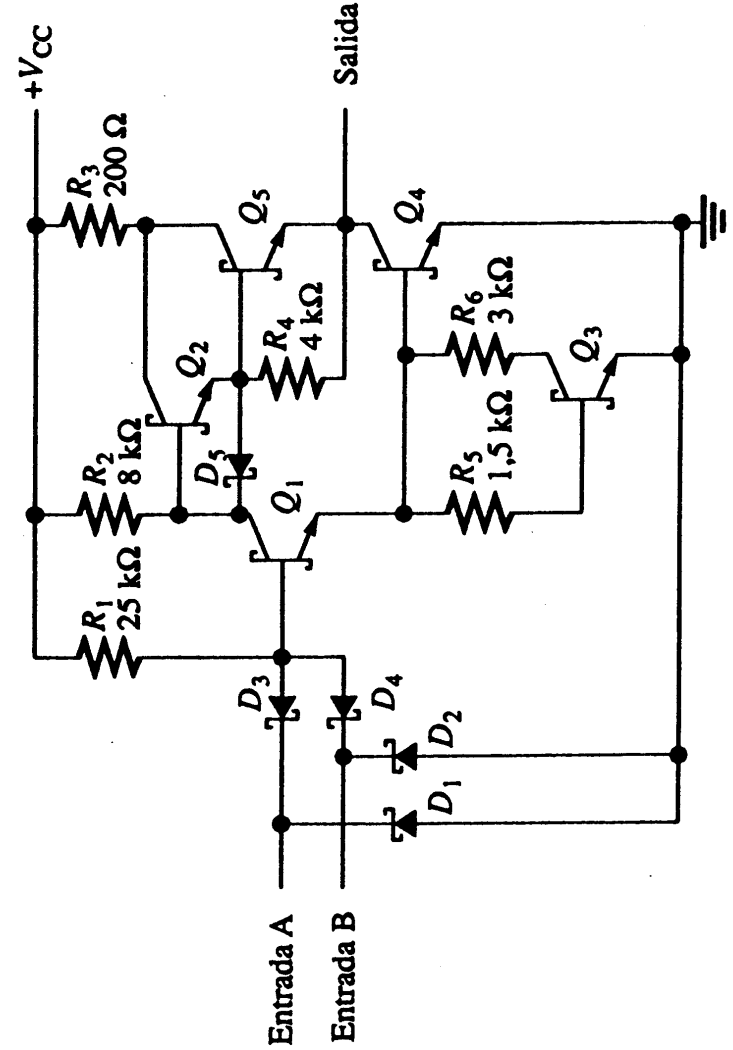




Puerta NOR TTL



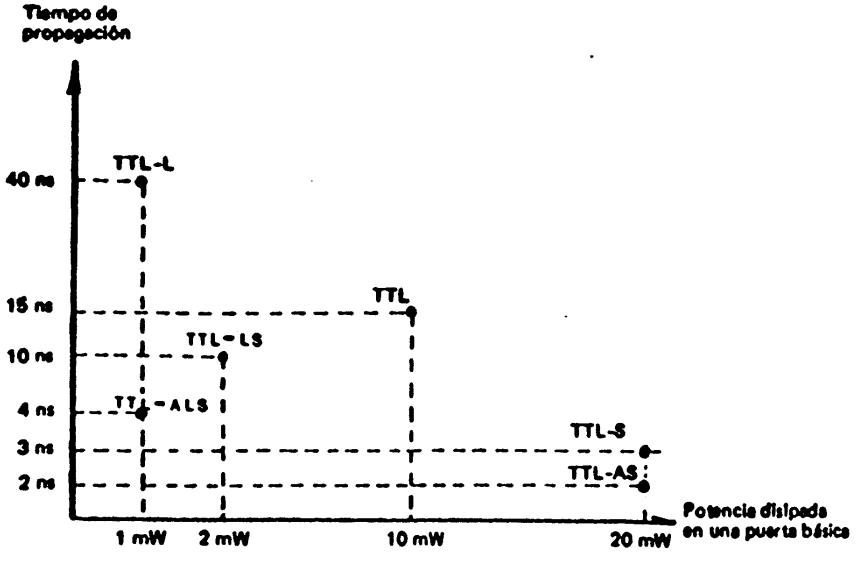
Puerta NAND TTL-LS



Otras Subfamilias

54/74XXXX	TTL ESTANDAR
54/74LXXXX	TTL DE BAJO CONSUMO
54/74LSXXXX	TTL SCHOTTKY DE BAJO CONSUMO
54/74ASXXXX	TTL SCHOTTKY AVANZADA
54/74ALSXXXX	TTL SCHOTTKY AVANZADA DE BAJO CONSUMO

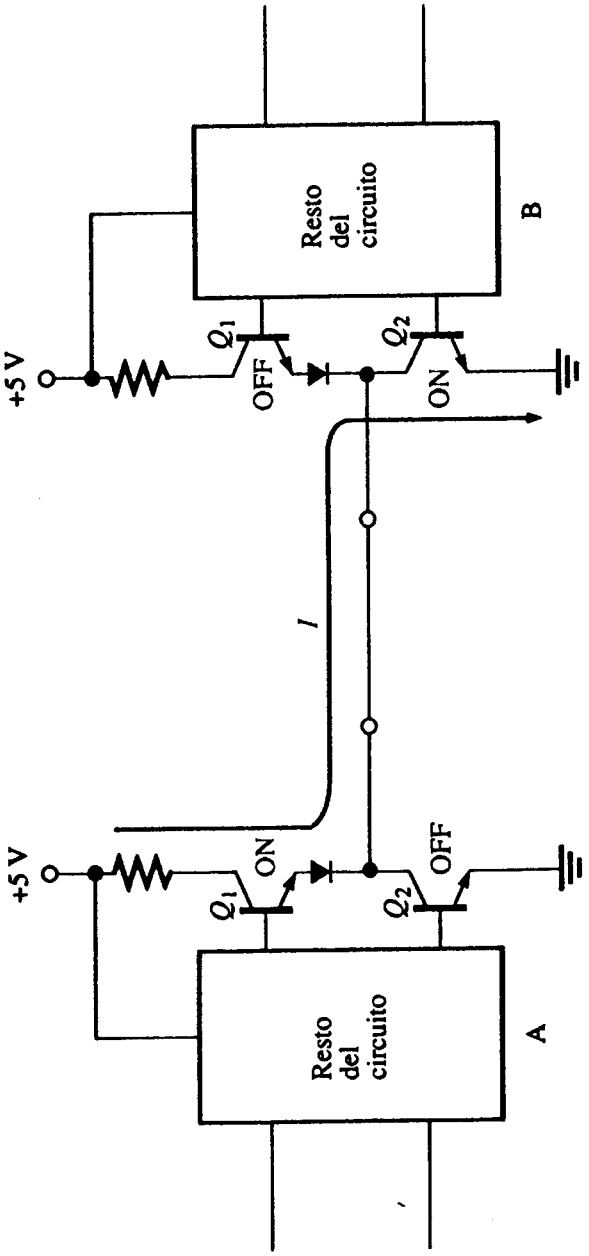
El "*producto retardo de propagación por potencia consumida*": Es un factor de mérito para cada tecnología



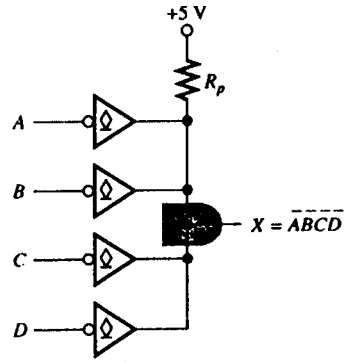
Unidad de carga

FAMILIA DE DISPOSITIVOS	CORRIENTE POR UNIDAD DE CARGA	CORRIENTE DE SALIDA
TTL	I_L=-1.6mA I_H=40µA	I_{OL}=16mA I_{OH}=-400µA
LOW POWER SCHOTTKY	I_L=-400µA I_H=20µA	I_{OL}=8mA I_{OH}=-400µA
ADVANCED LOW POWER SCHOTTKY	I_L=-100µA I_H=20µA	I_{OL}=8mA I_{OH}=-400µA
SCHOTTKY	I_L=-2mA I_H=50µA	I_{OL}=20mA I_{OH}=-1mA
ADVANCED SCHOTTKY	I_L=-500µA I_H=20µA	I_{OL}=20mA I_{OH}=-2mA
LOW POWER	I_L=-180µA I_H=10µA	I_{OL}=2mA I_{OH}=-200µA

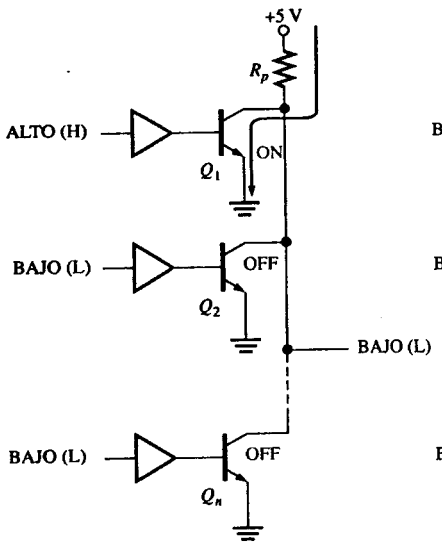
Conexión de las salidas totem-pole



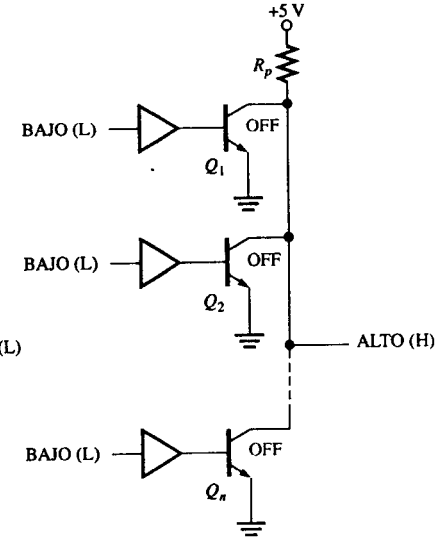
Puertas en colector abierto



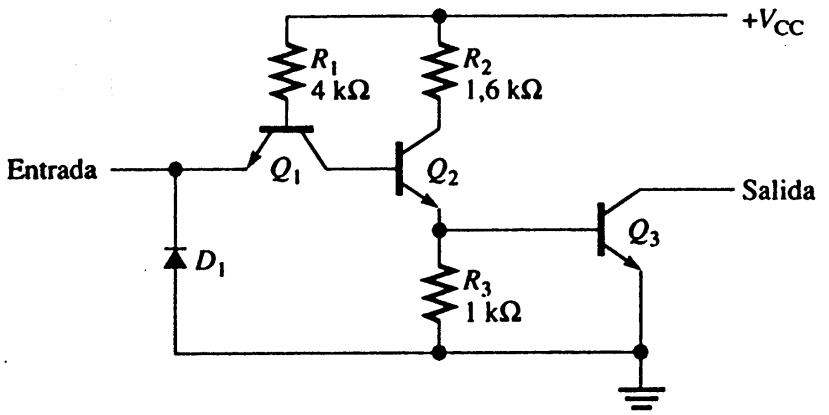
$$X = \overline{A}\,\overline{B}\,\overline{C}\,\overline{D}$$



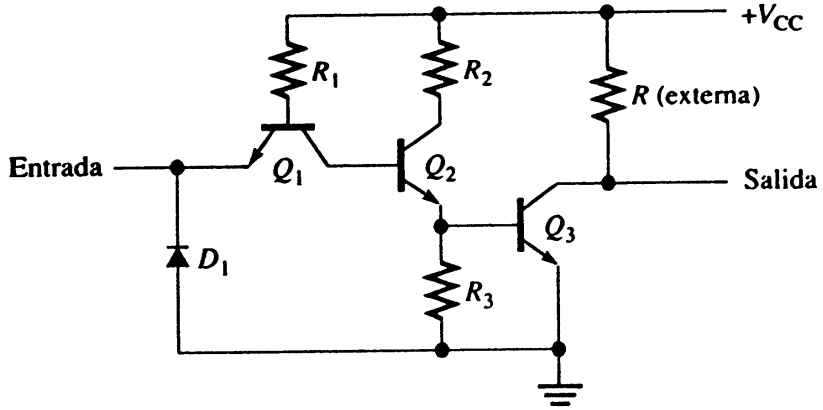
Cuando uno o más transistores de salida se saturan, la salida es un nivel bajo.



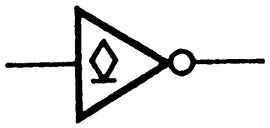
Cuando todos los transistores de salida están bloqueados, la salida es un nivel alto.



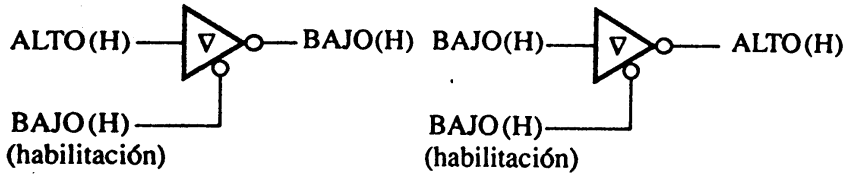
Circuito inversor con salida en colector abierto



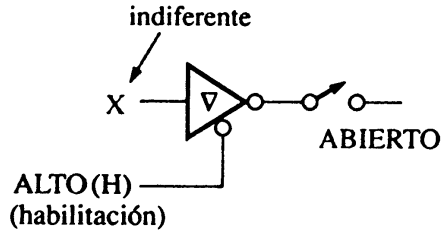
Con resistencia de pull-up externa



Puertas con salida triestado

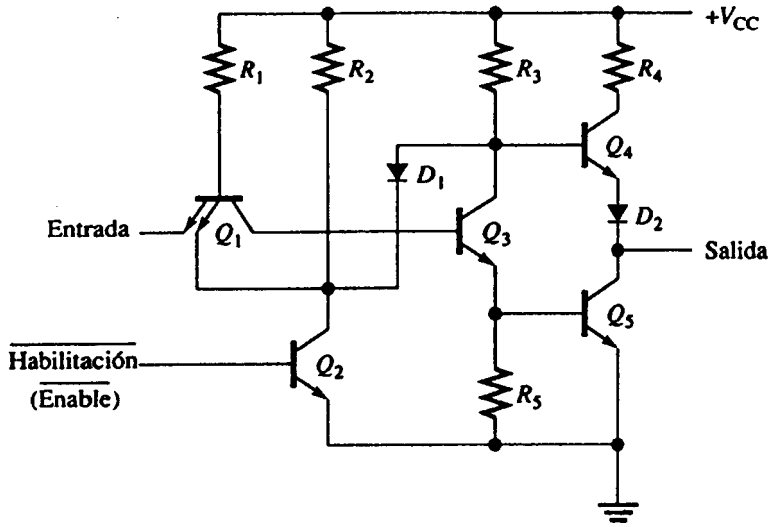


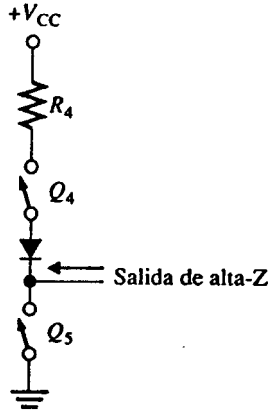
Habilitado para funcionamiento lógico normal



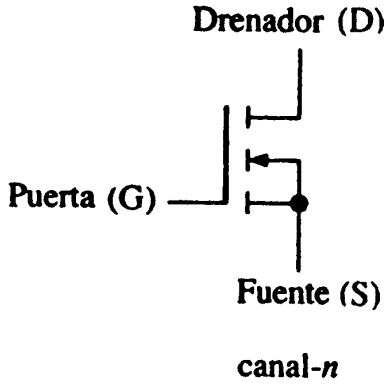
Estado de alta-Z

Circuito inversor Triestado

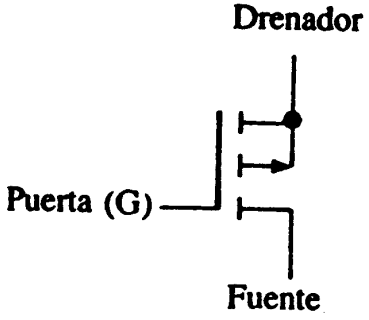




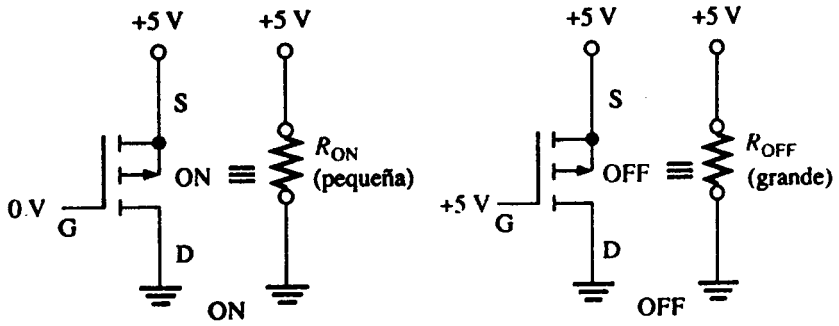
El MOSFET



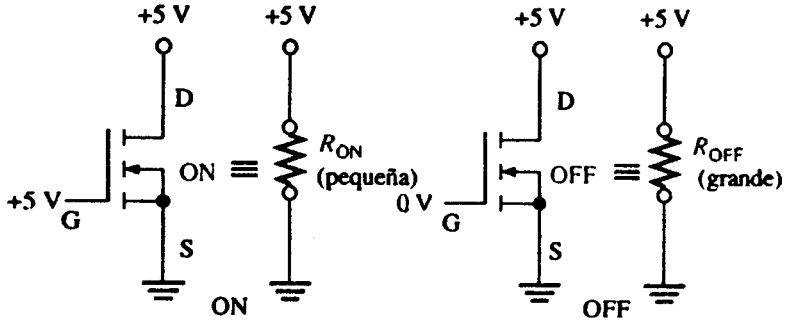
canal-*n*



canal-*p*

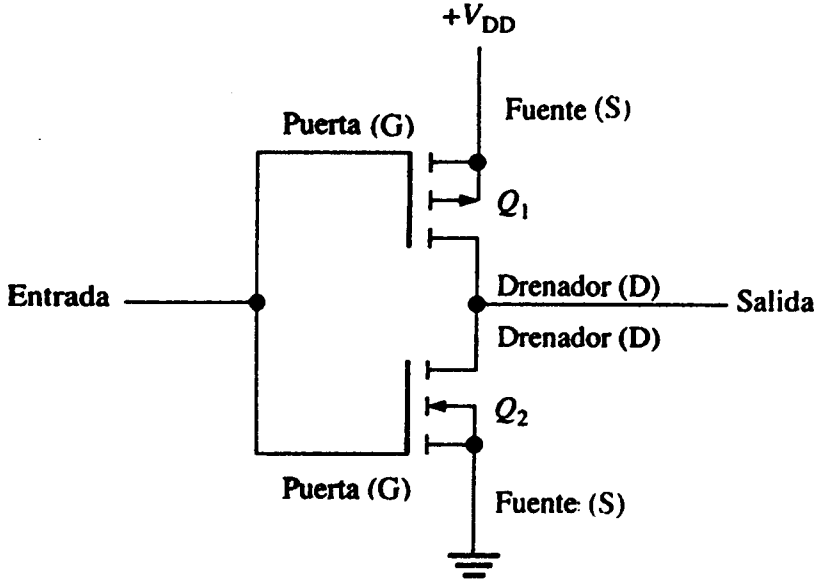


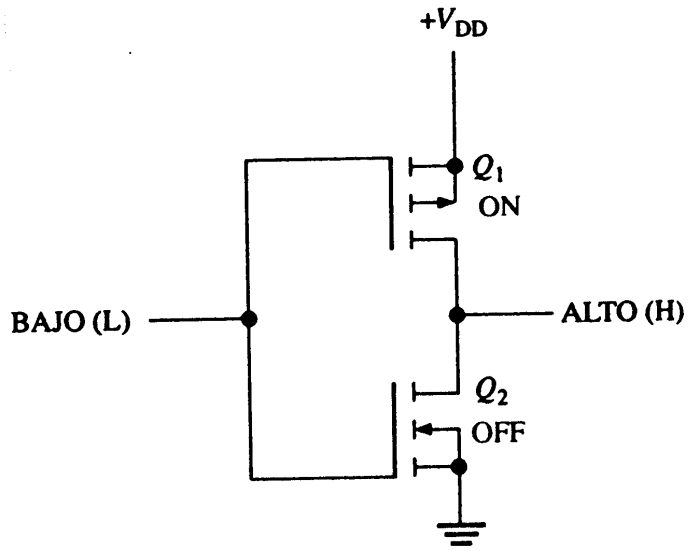
Interruptor canal-*p*

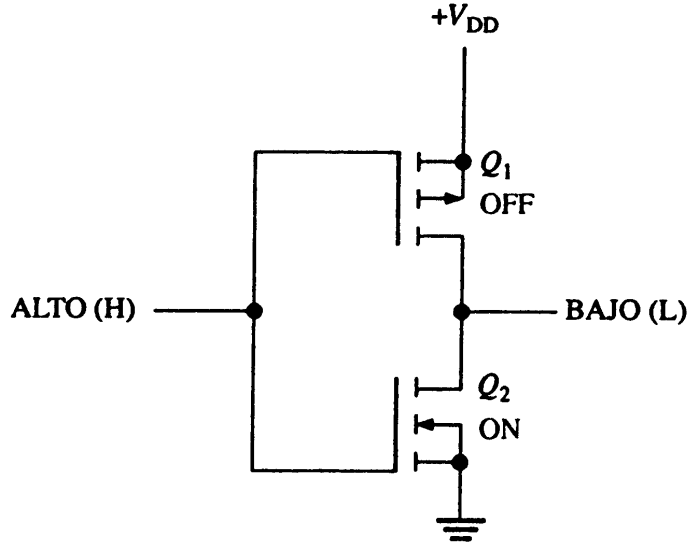


Interruptor canal-*n*

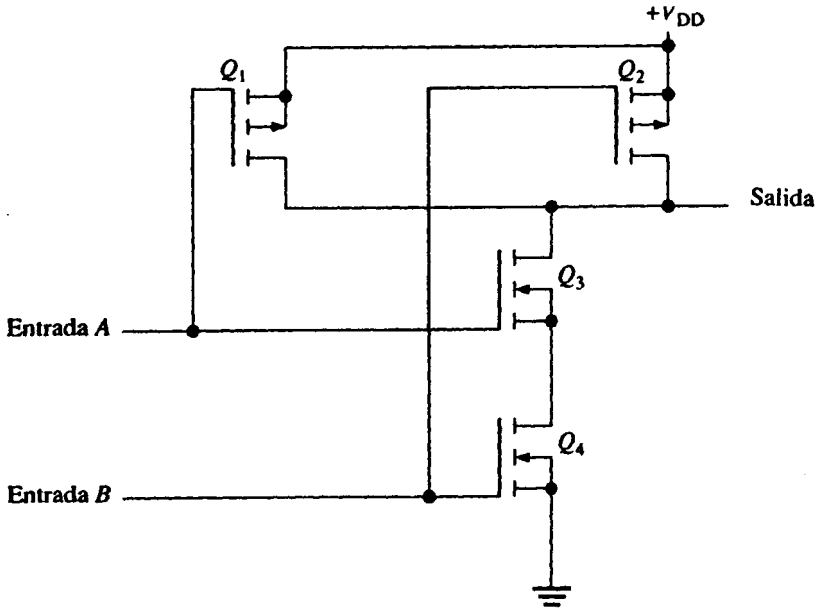
Inversor CMOS







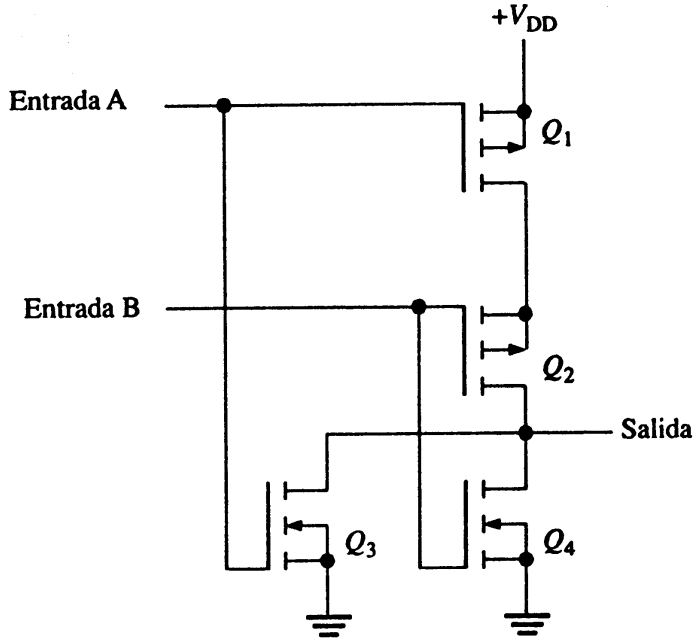
Puerta NAND-CMOS



A	B	Q_1	Q_2	Q_3	Q_4	X
L	L	S	S	C	C	H
L	H	S	C	C	S	H
H	L	C	S	S	C	H
H	H	C	C	S	S	L

C = corte (of)
S = saturación (on)
H = ALTO
L = BAJO

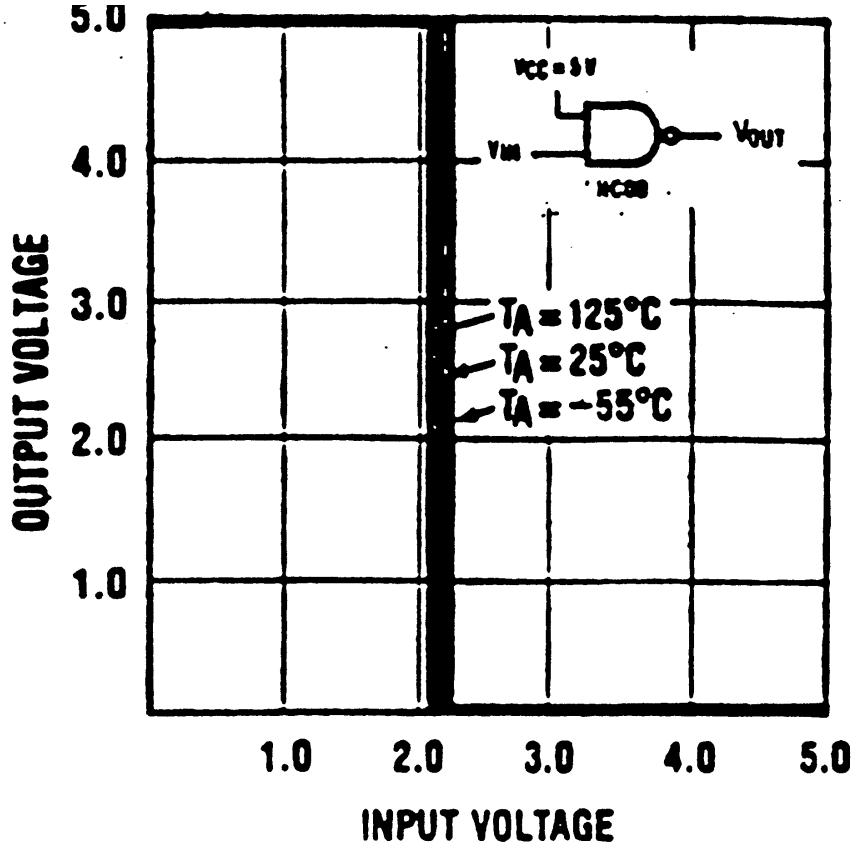
Puerta NOR-CMOS



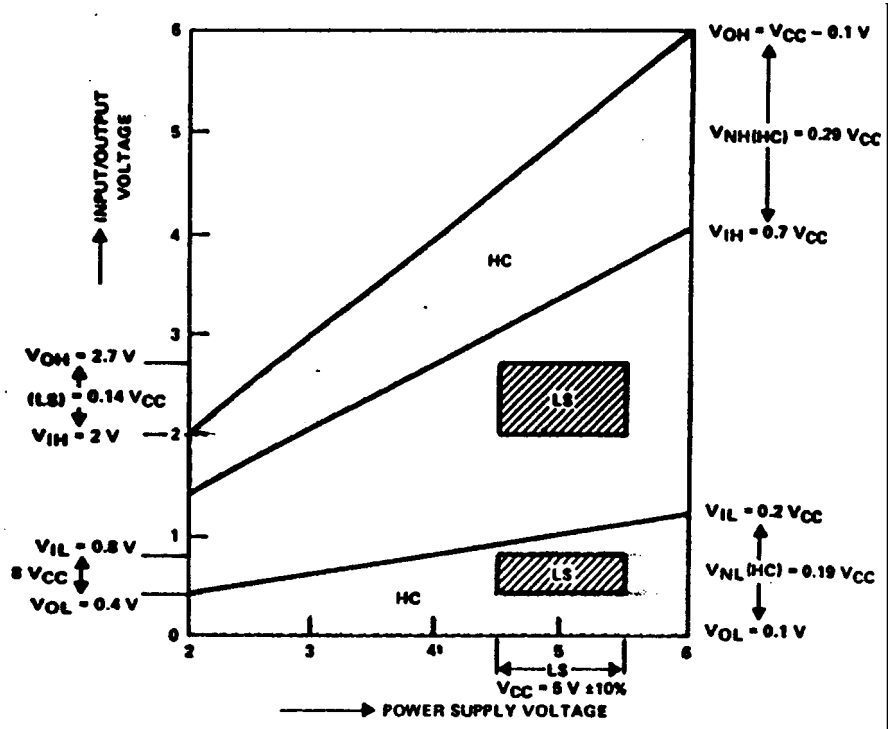
A	B	Q_1	Q_2	Q_3	Q_4	X
L	L	S	S	C	C	H
L	H	S	C	C	S	L
H	L	C	S	S	C	L
H	H	C	C	S	S	L

C= corte (off)
S= saturación (on)
H= ALTO
L= BAJO

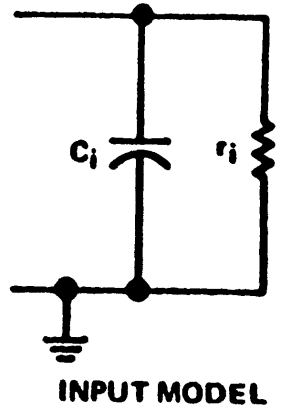
Característica de transferencia



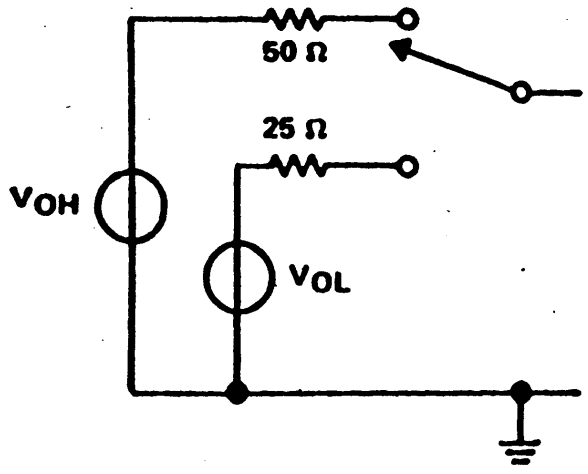
Niveles lógicos en función de la alimentación



Características de entrada salida



INPUT MODEL



OUTPUT MODEL

Puerta triestado

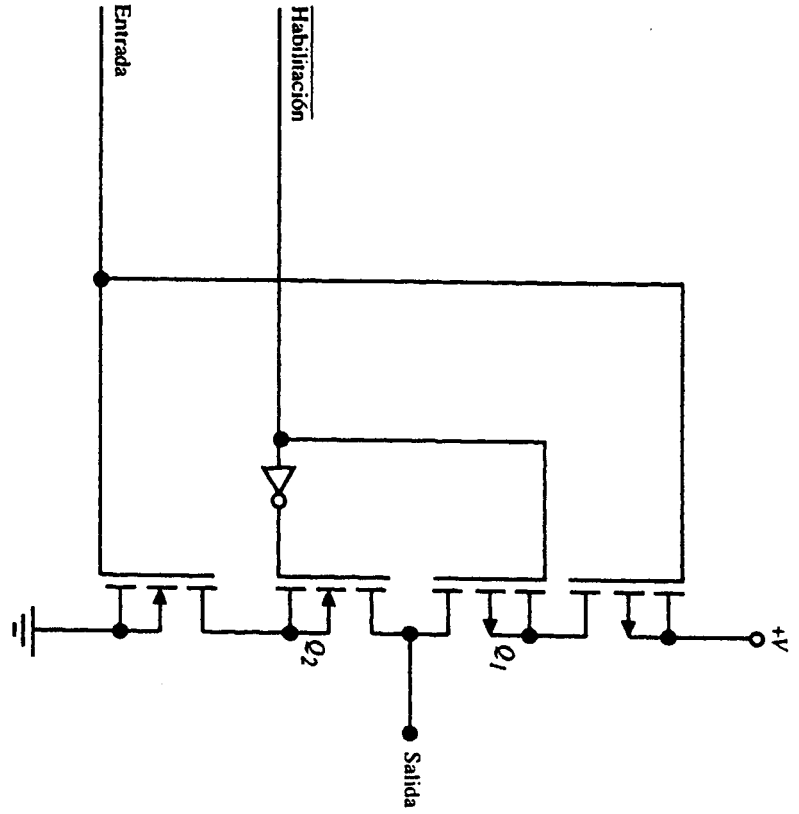


TABLA
Comparación de funcionamiento de las familias lógicas CMOS y TTL.

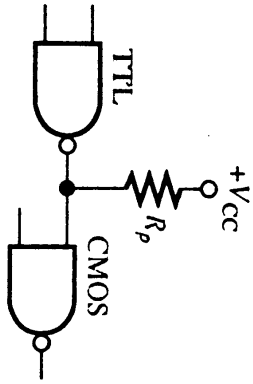
	CMOS		TTL				
Tecnología	**Puerta de silicio**	**Puerta de metal**	**Estándar**	**Schottky bajo consumo**	**Schottky**	**Schottky avanzada bajo consumo**	**Schottky avanzada**
Serie de dispositivos	74HC	4000	74	74LS	74S	74ALS	74AS
Disipación de potencia (mW/puerta):							
Estática	0,0000025	0,001	10	2	19	1	8,5
A100 kHz	0,17	0,1	10	2	19	1	8,5
Tiempo de retardo de programación (ns) (C_L = 15 pF)	8	50	10	10	3	4	1,5
Frecuencia máxima de reloj (MHz) (C_L = 15 pF)	40	12	35	40	125	70	200
Producto velocidad-potencia (pJ) (a 100 kHz)	1.4	11	100	20	57	4	13
Excitación de salida mínima I_{OL} (mA) (V_O = 0,4 V)	4	1.6	16	8	20	8	20
Fan-out:							
Carga LS	10	4	40	20	50	20	50
Misma-serie	*	*	10	20	20	20	40
Corriente de entrada máxima, I_{IL} (mA) (V_I = 0,4 V)	±0,001	−0,001	−1,6	−0,4	−2,0	−0,1	−0,5

* El fan-out depende de la frecuencia.

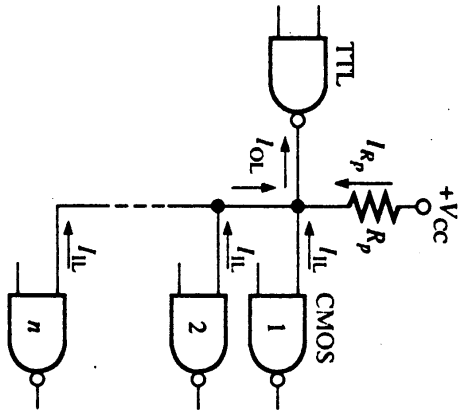
Interfaz entre las familias lógicas

Parámetro	74HC CMOS	74 TTL	74LS TTL	74S TTL	74AS TTL
$V_{IH(mín)}$	3,15 V	2 V	2 V	2 V	2 V
$V_{IL(máx)}$	1 V	0,8 V	0,8 V	0,8 V	0,8 V
$V_{OH(mín)}$	4,9 V	2,4 V	2,7 V	2,7 V	2,7 V
$V_{OL(máx)}$	0,1 V	0,4 V	0,4 V	0,5 V	0,5 V
$I_{IH(máx)}$	1 μA	40 μA	20 μA	50 μA	200 μA
$I_{IL(máx)}$	−1 μA	−1,6 mA	−400 μA	−2 mA	−2 mA
$I_{OH(máx)}$	−4 mA	−400 μA	−400 μA	−1 mA	−2 mA
$I_{OL(máx)}$	4 mA	16 mA	8 mA	20 mA	20 mA

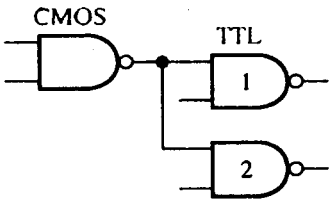
Interfaz TTL- CMOS



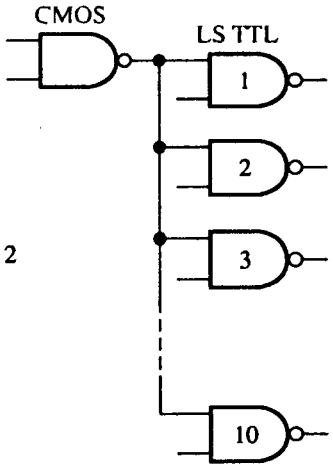
$$R_p = \frac{V_{CC} - V_{OL(mín)}}{I_{OL(TTL)} + nI_{IL(CMOS)}}$$



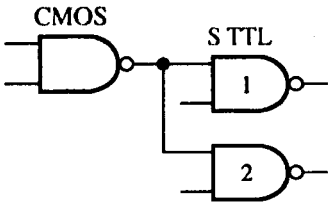
Interfaz CMOS-TTL



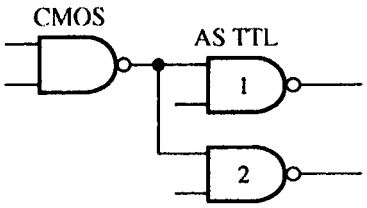
CMOS-TTL estándar. Fan-out = 2



CMOS-TTL Schottky de bajo consumo. Fan-out = 10

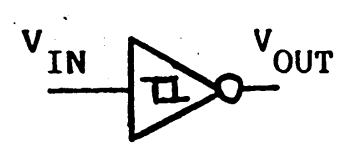


CMOS-TTL Schottky . Fan-out = 2

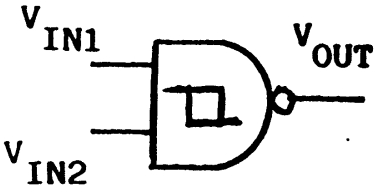


CMOS-TTL Schottky avanzada. Fan-out = 2

Puerta SCHMITT

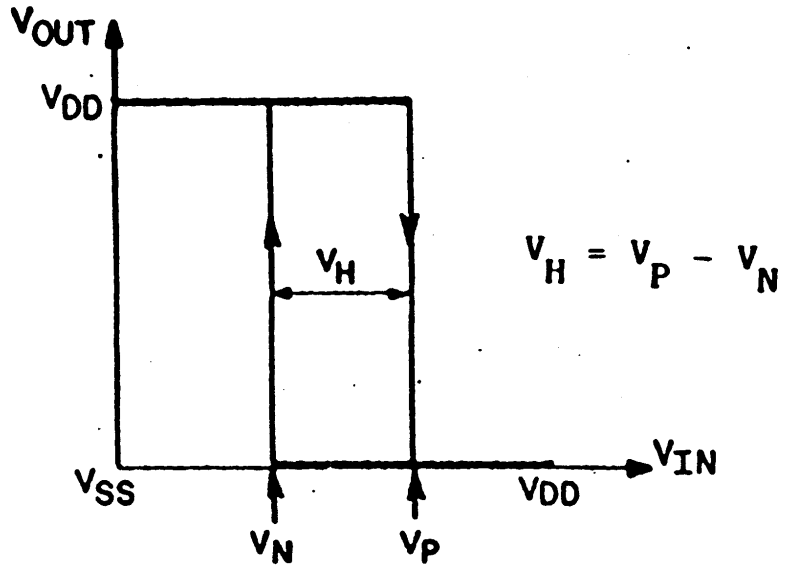


INVERSOR SCHMITT

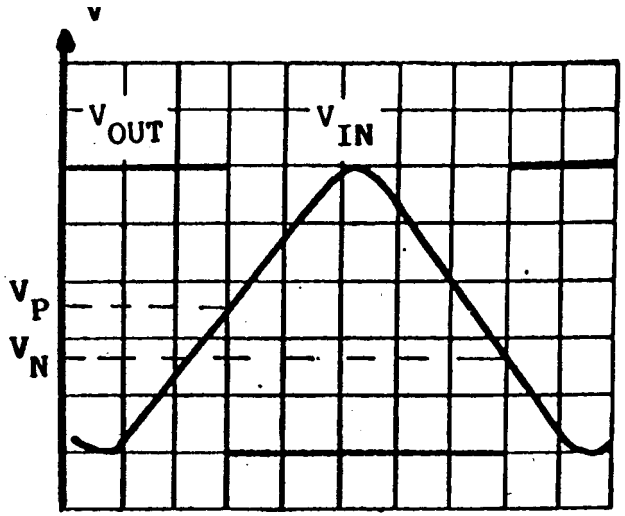


NAND SCHMITT

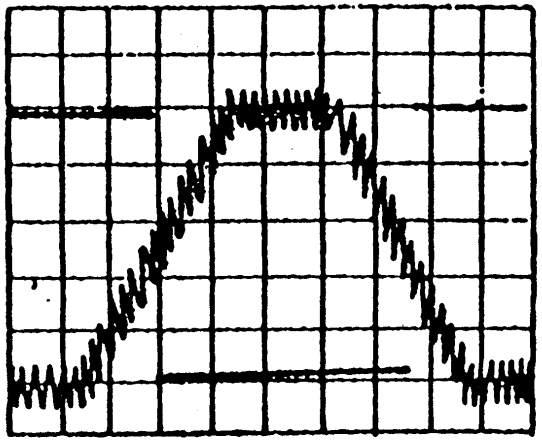
Característica de transferencia



Tiempos de subida/bajada

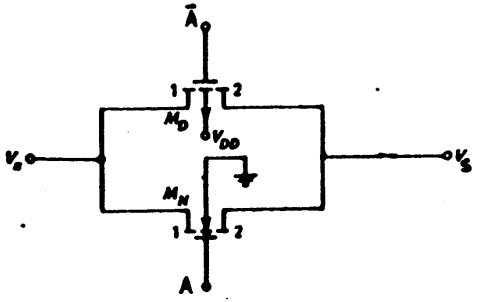


Tiempos de subida/bajada



Puertas de transmisión

Estructura y tabla de verdad



A	V_x	V_s
0	X	Z
1	V_x	V_x

Si A=0 la puerta está cerrada y $R_{eq} = 10^9$ oh.

Si A=1 la resistencia de la puerta varía dependiendo del valor de V_x